VINCULUM

BINDING USB TECHNOLOGIES

Future Technology Devices International Ltd.

V2-EVAL Revision 2

Vinculum II Evaluation Board Rev2

Datasheet

Document Reference No.: FT_000402

Version 2.0

Issue Date: 2015-03-23

Future Technology Devices International Ltd (FTDI)

Unit 1, 2 Seaward Place, Centurion Business Park, Glasgow, G41 1HH, United Kingdom

Tel.: +44 (0) 141 429 2777 Fax: + 44 (0) 141 429 2758

E-Mail (Support): support1@ftdichip.com

Web: http://www.vinculum.com

Table of Contents

1 Introduction

The following document details the features and specifications of the V2-EVAL board, Revision 2 of the PCB. This will be refered to as the V2-EVAL throughout the remainder of the datasheet. The V2-EVAL is a hardware platform designed to support easy evaluation of FTDI's Vinculum-II (VNC2) series of embedded USB host controller devices.

The V2-Eval kit includes the following hardware items as standard

- 1 x V2-Eval base board.
- 1 x 5V/1A mains adapter PSU – UK, US, European and Japanese versions available.
- 1 x USB A/B cable to connect to a host PC in programming / terminal emulation or debugging modes.
- 1 x USB gender changer for USB slave mode applications.

NOTE:

The V2-EVAL kit requires a VNC2 based daughterboard module to be installed into the V2-EVAL base board socket site, in order to enable development with the kit.

Daughterboard modules are sold separately, with 3 versions available for 32-pin, 48-pin and 64-pin package devices. Daughterboard modules can be purchased from FTDI or via our website http://www.ftdichip.com.

Daughterboards for V2-EVAL revision 1 are also used in the Revision 2 version of the PCB.

Before you proceed:
Please check that all the contents of the package are not damaged.

Ensure that your kit includes a proper version of the power supply, depending on the region where you live. Eval application software and project examples can be downloaded from: http://www.ftdichip.com

1.1 Handling the board

Static discharge precaution – Without proper anti-static handling the board can be damaged. Therefore, take anti-static precautions while handling the board.

1.2 Environmental requirements

The V2-Eval Board must be stored between -40°C and 80°C. The recommended operating temperature is between 0°C and 55°C

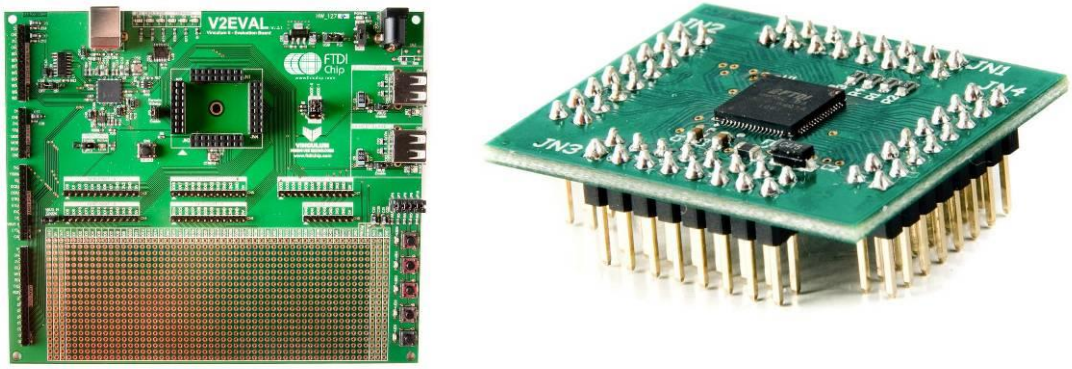


Figure 1.1 : V2-EVAL Motherboard(left) with Daughterboard Module(right)

1.3 Part Numbers

Part Number	Description
V2-EVAL	V2-EVAL kit with base board, power supply and cables.
V2-EVAL-EXT32	VNC2 daughterboard module with 32-pin QFN VNC2 device for use with V2-EVAL.
V2-EVAL-EXT48	VNC2 daughterboard module with 48-pin QFN VNC2 device for use with V2-EVAL.
V2-EVAL-EXT64	VNC2 daughterboard module with 64-pin QFN VNC2 device for use with V2-EVAL.

Table 1.0 : Part Numbers

1.4 References

The document contains references to the following websites and documents. Links to most documents are available from the FTDI website, http://www.ftdichip.com.

Document Name	Description
1. FT_000138	Vinculum-II Embedded Dual USB Host Controller IC Data Sheet.
2. FT_000060	FT4232H Data Sheet.
3. AN_135	MPSSE Basics
4. AN_137	Vinculum-II IO Cell Description.
5. AN_138	Vinculum-II Debug Interface Description.
6. AN_139	Vinculum-II IO Mux Explained.
7. AN_140	Vinculum-II PWM Example.
8. FT_000006	Vinculum Firmware User Manual.
9. USB 2.0	Universal Serial Bus Specification Revision 2.0 USB Implementers Forum http://www.usb.org.

Table 1.1 : Document References

1.5 Acronyms and Abbreviations

Terms	Description
FIFO	First In First Out.
GPIO	General Purpose Input Output.
I/O	Input / Output.
MISO	Master In Slave Out.
MOSI	Master Out Slave In.
MPSSE	Multi Purpose Synchronous Serial Engine
SPI	Serial Peripheral Interface.
UART	Universal Asynchronous Receiver/Transmitter.
USB	Universal Serial Bus.
VNC2	Vinculum-II.

Table 1.2 : Acronyms and Abbreviations

2 Board Description

V2-Eval Board is intended for use as a hardware platform to enable easy evaluation of FTDI's Vinculum-II VNC2 series of embedded USB Host / Slave controllers. The V2-Eval Board includes all the necessary components required by a user to begin developing USB Host / Slave system applications based on the VNC2 device.

2.1 V2-EVAL Board Features

- VNC2 – Embedded USB Host / Slave chip accessible via daughterboard.
- Selection of VNC2 daughterboards to support 32-pin, 48-pin and 64-pin QFN packages.
- Two USB type A connectors for connecting to USB slave peripherals.
- VNC2 IO port connectors grouped by port name/or function.
- FT42232H –USB to quad channel UART device for VNC2 programming & debug functions.
- One USB type B connector for connection to PC host via FT4232H.
- 4 User-programmable LEDs.
- 4 User-programmable push button switches.

2.2 Specifications

- Board supply voltage: 4.75V … 5.25V.
- Board supply current: 60mA (with no USB devices on USB1 or USB2 port).
- IO connectors power output: 5V/150mA, 3.3V/150mA.
- Base board dimensions: 167mm x 156mm x 1.5mm (L x W x H).
- VNC2 daughterboard dimensions: 37.9mm x 32.48mm x 10.0mm (L x W x H).

3 V2-Eval Board Components and Interfaces

This chapter describes the operational and connectivity information for the V2-Eval board major components and interfaces.

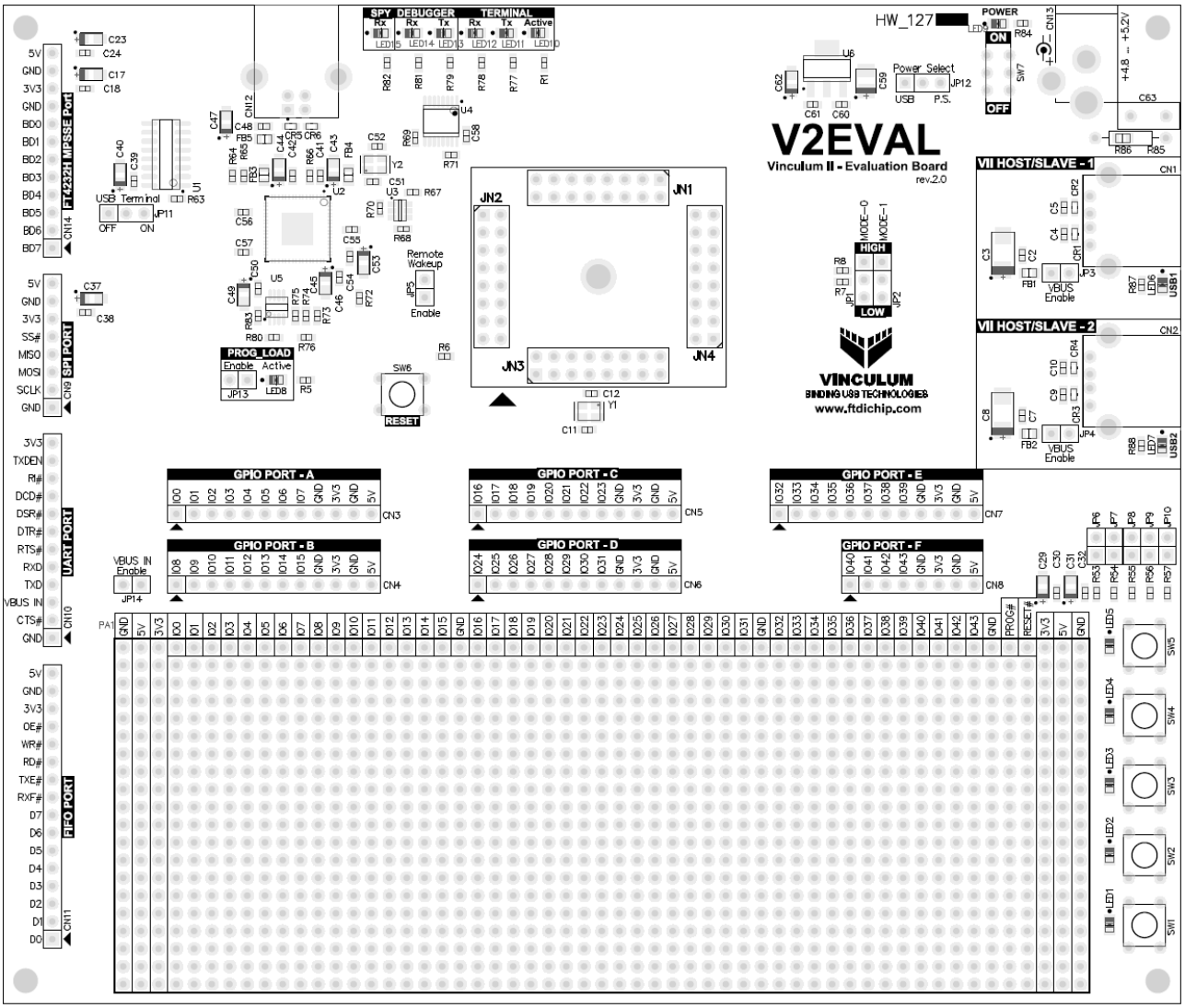


Figure 3.1 : V2-EVAL Board Layout

3.1 Block Diagram

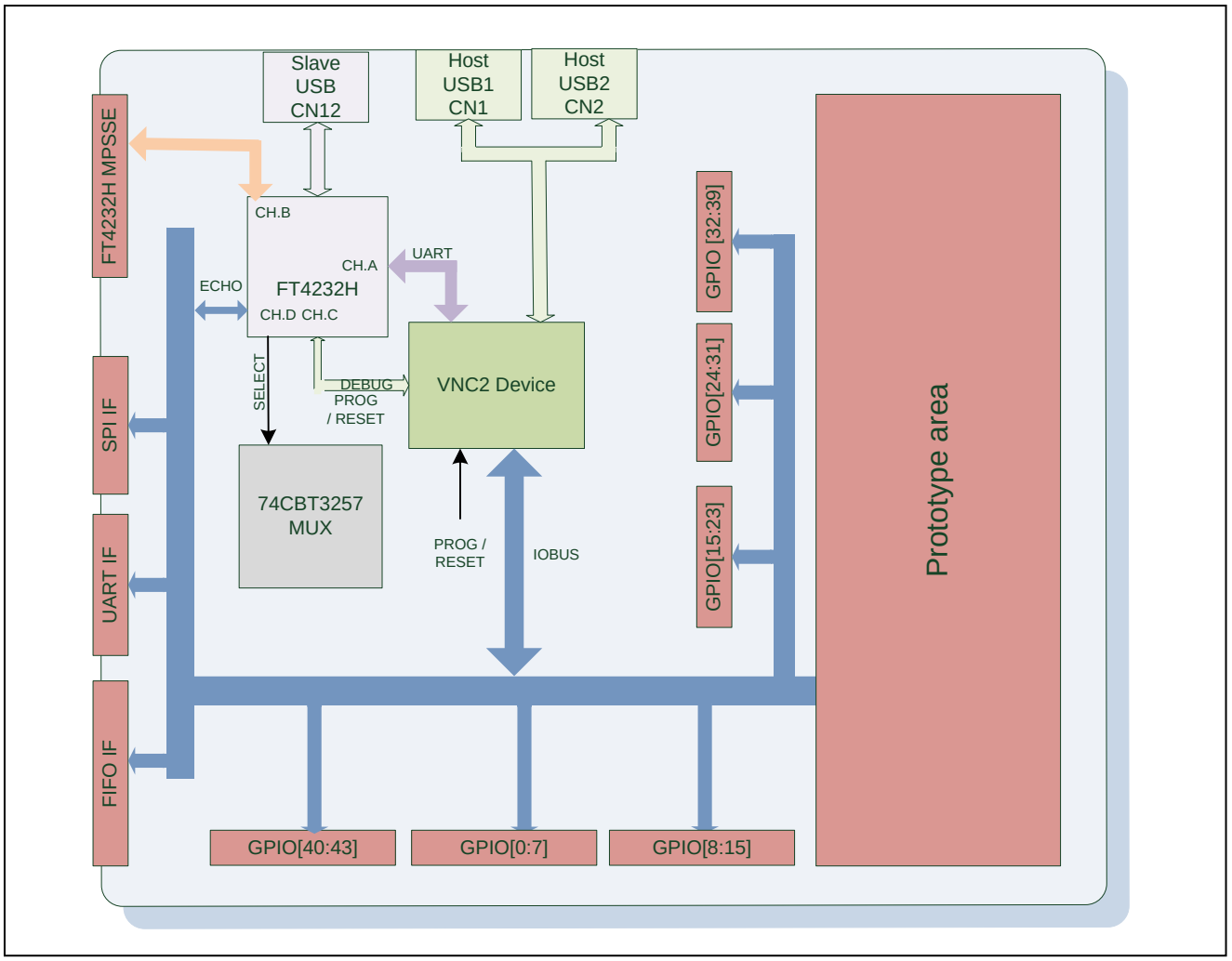


Figure 3.2 : V2-EVAL Board Block Diagram

3.1.1 Components.

Component	Board designator	Description
IO multiplexer	U1	74CBT3257 4-bit, 1to2, FET Multiplexer/Demultiplexer.
USB-UART bridge	U2	FT4232H USB ⇔ Quad UART/FIFO device.
Configuration memory	U3	9356 Serial SPI EEPROM for FT4232H configuration data.
Inverter	U4	SN74HCT595D 8 bit shifter to drive FT4232H UART traffic LEDs.
Dual port buffer	U5	SN74LVC2G241 dual port buffer used to convert bi-directional debug signal into separate TX and RX signals.
3.3V regulator	U6	AIC1735-33 Ultra low dropout 3.3V voltage regulator.
12MHz crystal	Y1	12MHz crystal for Daughterboard
12MHz crystal	Y2	12MHz crystal for FT4232H.
Single 5V DC power supply	CN13	Board adapter for included 5V DC power supply.
Keyboard	SW1-SW5	Four user push-button switches.
Reset button	SW6	Push-button switch for manual reset of VNC2 device.
Power switch	SW7	Power On/Off switch.
User LEDs	LED1-LED5	Five green user LEDs.
USB 1 Active	LED6	Green LED.
USB 2 Active	LED7	Green LED.
PROG LED	LED8	Red LED.
Power LED	LED9	Yellow LED.
USB Terminal Active	LED 10	Red LED
UART TX LED	LED11	Red LED.
UART RX LED	LED12	Green LED.
Debug TX	LED13	Red LED.
Debug RX	LED14	Green LED.
SPI_RX	LED15	Green LED.
GPIO I/O Jumpers	JP1, JP2	GPIO I/O jumpers .
VBUS jumpers	JP3, JP4	USB1, USB2 power bus enable jumpers.
REMOTE WAKEUP	JP5	VNC2 remote wakeup jumper.
LEDs enable jumpers	JP6-JP10	Enable/disable user-defined LEDs.
USB terminal	JP11	Enable/disable USB terminal port
Power source select	JP12	Power source selection jumper.

Table 3.1 : V2-Eval Board Components

3.1.2 Interfaces.

Component	Board designator	Description
USB1, USB2 (1)	CN1, CN2	VNC2 USB host ports 1&2.
USB Type B	CN12	FT4232H USB Slave connection.
VNC2 Socket	JN1 -JN4	Daughterboard connectors for VNC2 Daughterboard.
SPI (2)	CN9	VNC2 SPI interface pins.
UART (2)	CN10	VNC2 UART interface pins.
FIFO (2)	CN11	VNC2 FIFO interface pins.
IOBUS[7..0] (2)	CN3	VNC2 IOBUS [7:0] port pins.
IOBUS[8..15] (2)	CN4	VNC2 IOBUS [8:15] port pins.
IOBUS[16..23] (2)	CN5	VNC2 IOBUS [16:23] port pins.
IOBUS[24..31] (2)	CN6	VNC2 IOBUS [24:31] port pins.
IOBUS[32..39] (2)	CN7	VNC2 IOBUS [32:39] port pins.
IOBUS[40..43] (2)	CN8	VNC2 IOBUS [40:43] port pins.
Prototyping area (2)	PA1	All of VNC2 IO ports and PROG#, RESET# pins are brought on to this area.

Notes

(1) Gender changer required when ports are configured as slave ports by VNC2 firmware, to enable connection to a USB host port.

(2) Those pins are shared between different areas and connectors on the board. You can use only one device at time connected to those pins.

Table 3.2 : V2-Eval Board Interfaces

4 Initial Board Set-up & Test

4.1 Installing VNC2 Daughterboard

Prior to first powering the board, users must ensure that the daughterboard module hosting the VNC2 chip is correctly installed on to the main V2-Eval board. The V2-Eval board has 4 socket connectors, JN1-JN4, onto which the VNC2 daughterboard module is installed.

On the VNC2 daughterboard module, connector JN1 connects to corresponding socket JN1, JN2 connects to socket JN2, JN3 connects to socket JN3 and JN4 connects to JN4 on the V2-Eval board.

Warning!

Please check that the VNC2 daughterboard module is correctly installed onto the V2-Eval board prior to power-up. Incorrect installation can cause the VNC2 to not function.

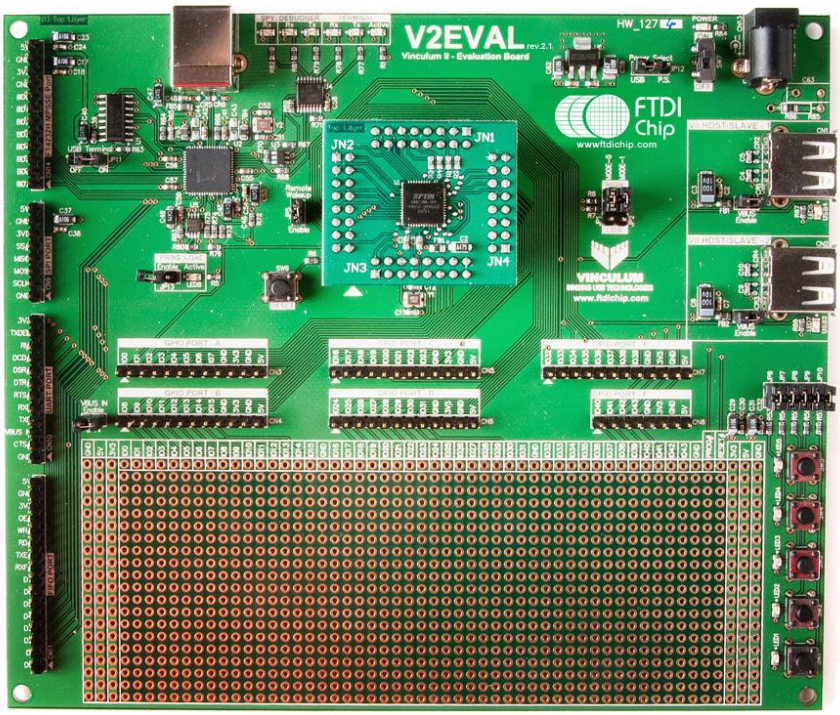


Figure 4.1 : V2-EVAL Board with VNC2 Daughterboard Installed

4.2 Testing the board.

Ensure that the Power Select jumper JP12 is in 'P.S.' position (pins 2 & 3 shorted), to enable the board to be powered from the external power adapter.

Connect the 5V DC/1A power supply included in V2-Eval Kit to the external input power adapter connector (CN13), connect USB A/B cable to USB B connector (CN12) on V2-Eval Board and to a free USB port on host PC. Switch SW7 to the ON position (towards board edge). LED9 – POWER should now be on.

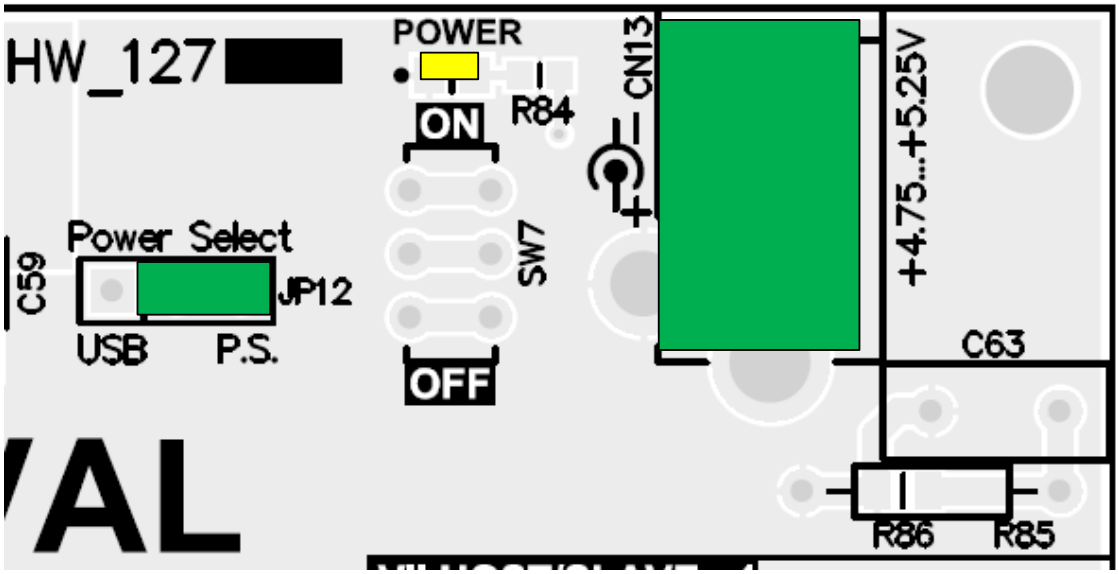


Figure 4.2 : Power connector with Jumper JP2

The PCB circuitry will draw power either directly from the board 5V supply or from a 3.3V regulator that is powered by this 5V supply. This includes the VNC2 daughterboard module that is installed on the board. Upon power up, the power LED (LED9) will illuminate.

5 Detailed Description of Board Components.

5.1 Power Select Jumper JP12.

Figure 5.1 : Power Select Jumper Configuration for USB Power

V2-Eval Board can draw its power either from the external 5V/1A DC Power Supply or from the USB interface when connected to a USB host via the B type connector (CN12). To enable USB power supply feature, switch the jumper JP12 to USB position, pins 1&2 shorted (pin 1 has a rectangle shaped pad on the bottom side of the board).

Warning!

Please remember that every device connected to the PC through USB port can draw NO MORE than 500mA from the USB host PC 5V power bus.

5.2 GPIO BUS Connectors

The V2-EVAL board features a set of 6 connectors providing access to GPIO capable pins on the VNC2 device. The GPIO pins are distributed across 6 connectors. The configuration of each connector is outlined in subsequent sections. Further each connector has a 5V and 3.3V power and GND pins.

5.2.1 GPIO [0:7] Connector CN3

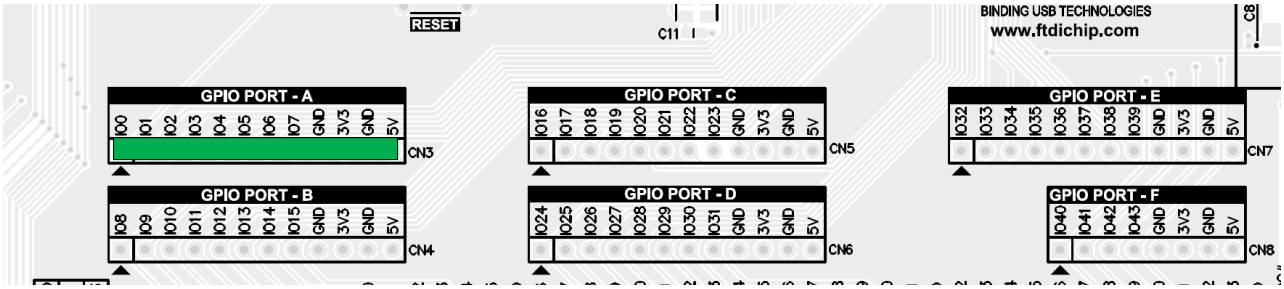


Figure 5.2 : GPIO[0:7] Connector CN3

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
IO0 (3)	1	11	11	11	IO	GPIO data bit 0
IO1 (3)	2	12	12	12	IO	GPIO data bit 1
IO2 (3)	3	14	13	13	IO	GPIO data bit 2
IO3 (3)	4	15	14	14	IO	GPIO port, data bit 3
IO4 (3)	5	-	-	15	IO	GPIO port, data bit 4
IO5 (3)	6	-	-	16	IO	GPIO port, data bit 5
IO6 (3)	7	-	-	17	IO	GPIO port, data bit 6
IO7 (3)	8	-	-	18	IO	GPIO port, data bit 7
GND	9	-	-	-	-	Ground pin
3V3(4)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(5)	12	-	-	-	-	5V power rail.

Notes:

(3) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels.
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(4) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(5) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.1 : GPIO[0:7] port connector CN3

5.2.2 GPIO [8:15] Connector CN4

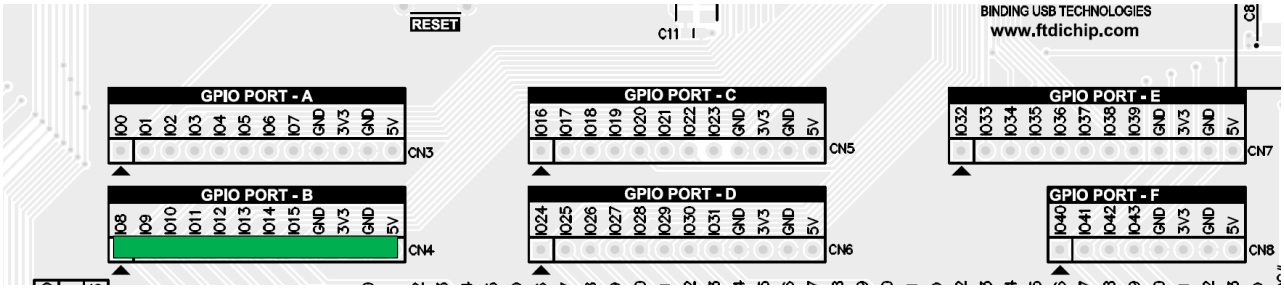


Figure 5.3 : GPIO[8:15] Connector CN4

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
IO8 (6)	1	-	-	19	IO	GPIO port, data bit 8
IO9 (6)	2	-	-	20	IO	GPIO port, data bit 9
IO10 (6)	3	-	-	22	IO	GPIO port, data bit 10
IO11 (6)	4	-	-	23	IO	GPIO port, data bit11
IO12 (6)	5	-	-	24	IO	GPIO port, data bit 12
IO13 (6)	6	-	-	25	IO	GPIO port, data bit 13
IO14 (6)	7	-	-	26	IO	GPIO port, data bit 14
IO15 (6)	8	-	-	27	IO	GPIO port, data bit 15
GND	9	-	-	-	-	Ground pin
3V3(7)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(8)	12	-	-	-	-	5V power rail.

Notes:

(6) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(7) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(8) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.2 : GPIO[8:15] connector CN4

5.2.3 GPIO [16:23] Connector CN5

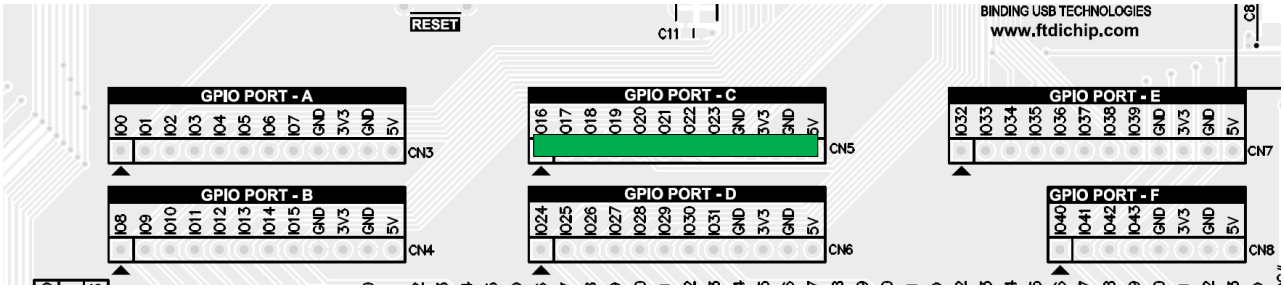


Figure 5.4 : GPIO[16:23] Connector CN5

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
IO16 (9)	1	-	-	27	IO	GPIO port, data bit 16
IO17 (9)	2	-	46	28	IO	GPIO port, data bit 17
IO18 (9)	3	-	45	29	IO	GPIO port, data bit 18
IO19 (9)	4	-	48	31	IO	GPIO port, data bit19
IO20 (9)	5	23	31	32	IO	GPIO port, data bit 20
IO21 (9)	6	24(10)	32(10)	39	IO	GPIO port, data bit 21
IO22 (9)	7	25	33	40	IO	GPIO port, data bit 22
IO23 (9)	8	26(10)	34 (10)	41	IO	GPIO port, data bit 23
GND	9	-	-	-	-	Ground pin
3V3(11)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(12)	12	-	-	-	-	5V power rail.

Notes:

(9) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(10) The following pins are only accessible on VNC2 when the onboard multiplexer select input is high. See section 6.4 for details.

(11) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(12) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.3 : GPIO port connector CN5

5.2.4 GPIO [24:31] Connector CN6

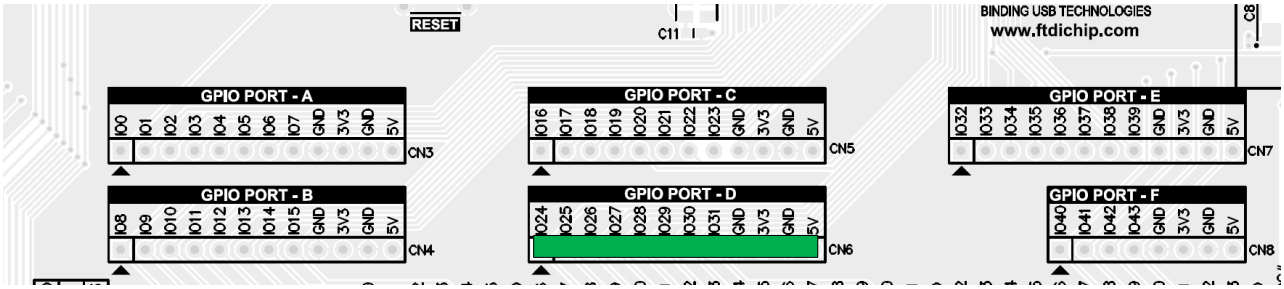


Figure 5.5 : GPIO[24:31] Connector CN6

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
IO24 (13)	1	-	35	43	IO	GPIO port, data bit 24
IO25 (13)	2	-	36	44	IO	GPIO port, data bit 25
IO26 (13)	3	-	37	45	IO	GPIO port, data bit 26
IO27 (13)	4	-	38	46	IO	GPIO port, data bit 27
IO28 (13)	5	-	41	47	IO	GPIO port, data bit 28
IO29 (13)	6	-	42	48	IO	GPIO port, data bit 29
IO30 (13)	7	-	43	49	IO	GPIO port, data bit 30
IO31 (13)	8	-	44	50	IO	GPIO port, data bit 31
GND	9	-	-	-	-	Ground pin
3V3(14)	10		-	-	-	3.3V power rail.
GND	11		-	-	-	Ground pin
5V(15)	12		-	-	-	5V power rail.

Notes:

(13) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(14) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(15) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB bus.

Table 5.4 : GPIO port connector CN6

5.2.5 GPIO [32:39] Connector CN7

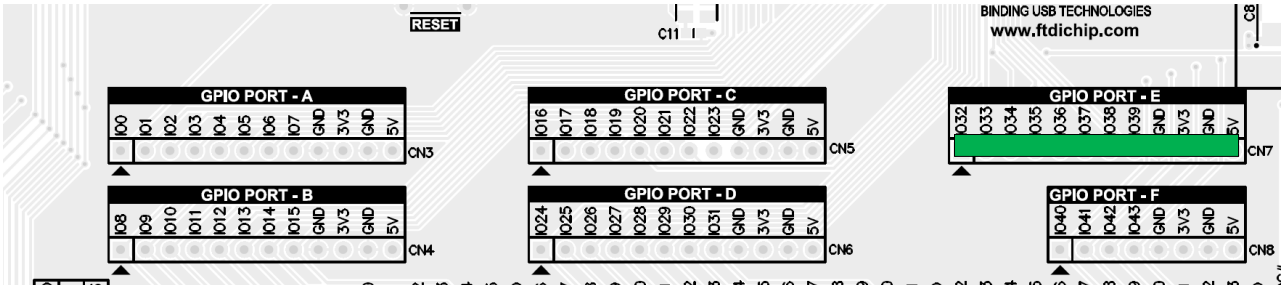


Figure 5.6 : GPIO[32:39] Connector CN7

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
IO32 (16)	1	29	15	51	IO	GPIO port, data bit 32
IO33 (16)	2	30	16	52	IO	GPIO port, data bit 33
IO34 (16)	3	31	18	55	IO	GPIO port, data bit 34
IO35 (16)	4	32	19	56	IO	GPIO port, data bit 35
IO36 (16)	5	-	-	57	IO	GPIO port, data bit 36
IO37 (16)	6	-	-	58	IO	GPIO port, data bit 37
IO38 (16)	7	-	-	59	IO	GPIO port, data bit 38
IO39 (16)	8	-	-	60	IO	GPIO port, data bit 39
GND	9	-	-	-	-	Ground pin
3V3(17)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(18)	12	-	-	-	-	5V power rail.

Notes:

(16) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(17) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(18) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

Table 5.5 : GPIO port connector CN7

5.2.6 GPIO [40:43] Connector CN8

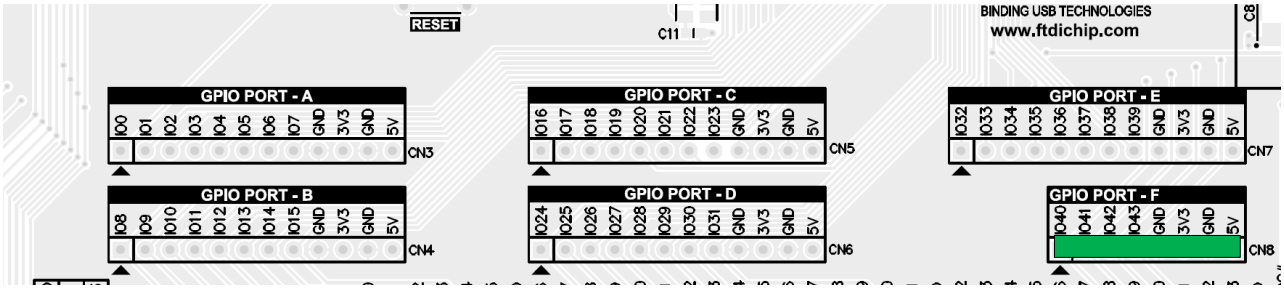


Figure 5.7 : GPIO[32:39] Connector CN8

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
IO40 (19)	1	-	20	61	IO	GPIO port, data bit 40
IO41 (19)	2	-	21	62	IO	GPIO port, data bit 41
IO42 (19)	3	-	22	63	IO	GPIO port, data bit 42
IO43 (19)	4	-	23	64	IO	GPIO port, data bit 43
GND	5	-	-	-	-	Ground pin
3V3(20)	6	-	-	-	-	3.3V power rail.
GND	7	-	-	-	-	Ground pin
5V(21)	8	-	-	-	-	5V power rail.

Notes:

(19) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(20) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(21) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.6 : GPIO port connector CN8

5.3 SPI Connector CN9

Table 5.7 details connector pinout for the SPI connector C9. A full description of each signal is available in the VNC2 data sheet.

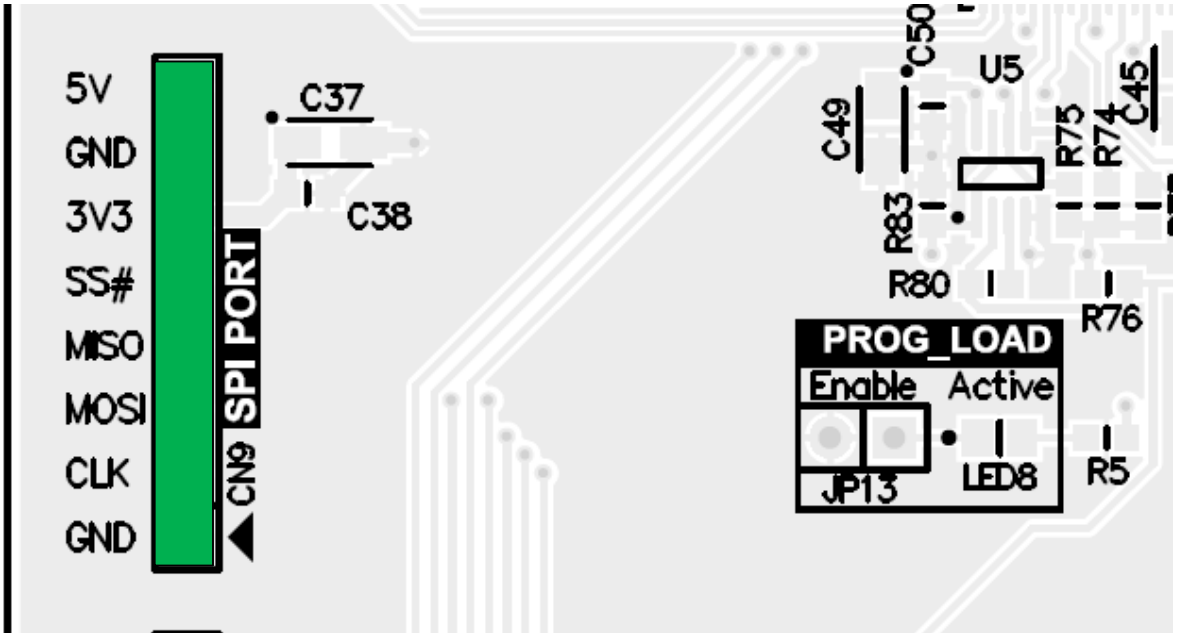


Figure 5.8 : SPI Connector CN9

Signal name	Connector pin	VCN2 Pin No		IO type	Description
		48-PIN	64-PIN		
GND	1	-	-	-	Ground pin
CLK (22)	2	31	39	Output	SPI CLK Input (IO20)
MOSI (22)	3	32	40	Output	SPI Master out slave in (IO21)
MISO(22)	4	33	41	Input	SDI Master in slave out (IO22)
SS# (22)	5	34	42	Output	Active low slave chip select 0 from master to slave 0 (IO23)
3V3(23)	6	-	-	-	3.3V power rail.
GND	7	-	-	-	Ground pin
5V(24)	8	-	-	-	5V power rail.

Notes:
Assumes SPI Master mode else signal directions change.

(22) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels.
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(23) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(24) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.7 : SPI Port Connector CN9

5.4 UART Interface Connector CN10

Table 5.8 details connector pinout for the UART connector CN10. A full description of each signal is available in the VNC2 data sheet.

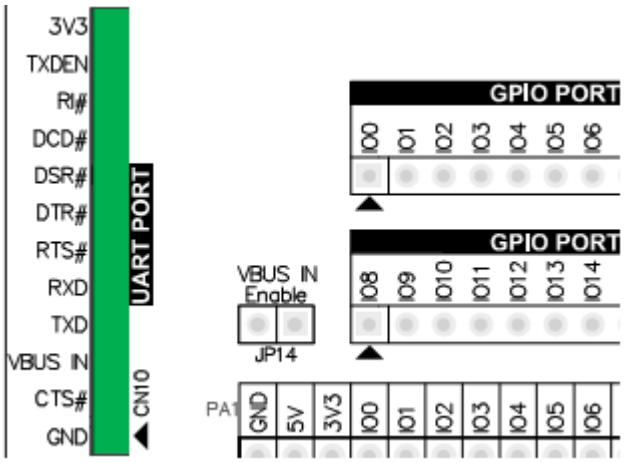


Figure 5.9 : UART Connector CN10

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GND	1		-	-	-	Ground pin
CTS# (25)	2	26(26)	34(26)	42	Input	Clear to Send Input / Handshake signal.
VBUS IN(28)	3		-	-	-	5V power rail.
TXD (25)	4	23	31	39	Output	Transmit data
RXD (25)	5	24(26)	32(26)	40	Input	Receive data
RTS# (25)	6	25	33	41	Output	Request to Send Control Output / Handshake signal.
DTR# (25)	7		35	43	Output	Data Terminal Ready Output / Handshake signal.
DSR# (25)	8		36	44	Input	Data Set Ready Input / Handshake signal.
DCD# (25)	9		37	45	Input	Data Carrier Detect Control Input
RI# (25)	10		38	46	Input	Ring Indicator Control Input
TXDEN#(25)	11		41	47	Output	Transmit Data Enable
3V3(27)	12		-	-	-	3.3V power rail.

Notes:

(25) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels..
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(26) The following pins are only accessible on VNC2 when the onboard multiplexer select input is high. See section 6.4 for details.

(27) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

(28) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

Table 5.8 : UART Interface Connector CN10

5.5 FIFO Interface Connector CN11

Table 5.9 details connector pinout for the FIFO connector CN11. A full description of each signal is available in the VNC2 data sheet.

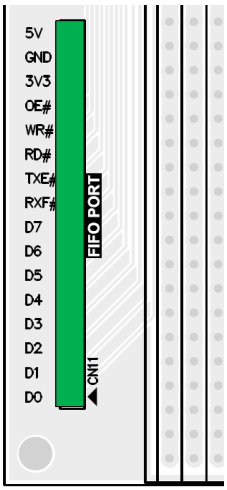


Figure 5.10 : FIFO Connector CN11

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
D0 (29)	1	-	31	39	IO	FIFO data bit 0, bidirectional
D1 (29)	2	-	32	40	IO	FIFO data bit 1, bidirectional
D2 (29)	3	-	33	41	IO	FIFO data bit 2, bidirectional
D3 (29)	4	-	34	42	IO	FIFO data bit 3, bidirectional
D4 (29)	5	-	35	43	IO	FIFO data bit 4, bidirectional
D5 (29)	6	-	36	44	IO	FIFO data bit 5, bidirectional
D6 (29)	7	-	37	45	IO	FIFO data bit 6, bidirectional
D7 (29)	8	-	38	46	IO	FIFO data bit 7, bidirectional
RXF#	9	-	41	47	Output	FIFO receive full output
TXE#	10	-	42	48	Output	FIFO transmitter buffer empty output
RD#	11	-	43	49	Input	FIFO read enable input
WR#	12	-	44	50	Input	FIFO write enable input
OE#	13	-	15	51	Input	FIFO output enable – synchronous FIFO only
3V3(30)	14	-	-	-	-	3.3V power rail.
GND	15	-	-	-	-	Ground pin
5V(31)	16	-	-	-	-	5V power rail.

Notes:

(29) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(30) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(31) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.9 : FIFO Interface Connector CN11

5.6 Prototyping area

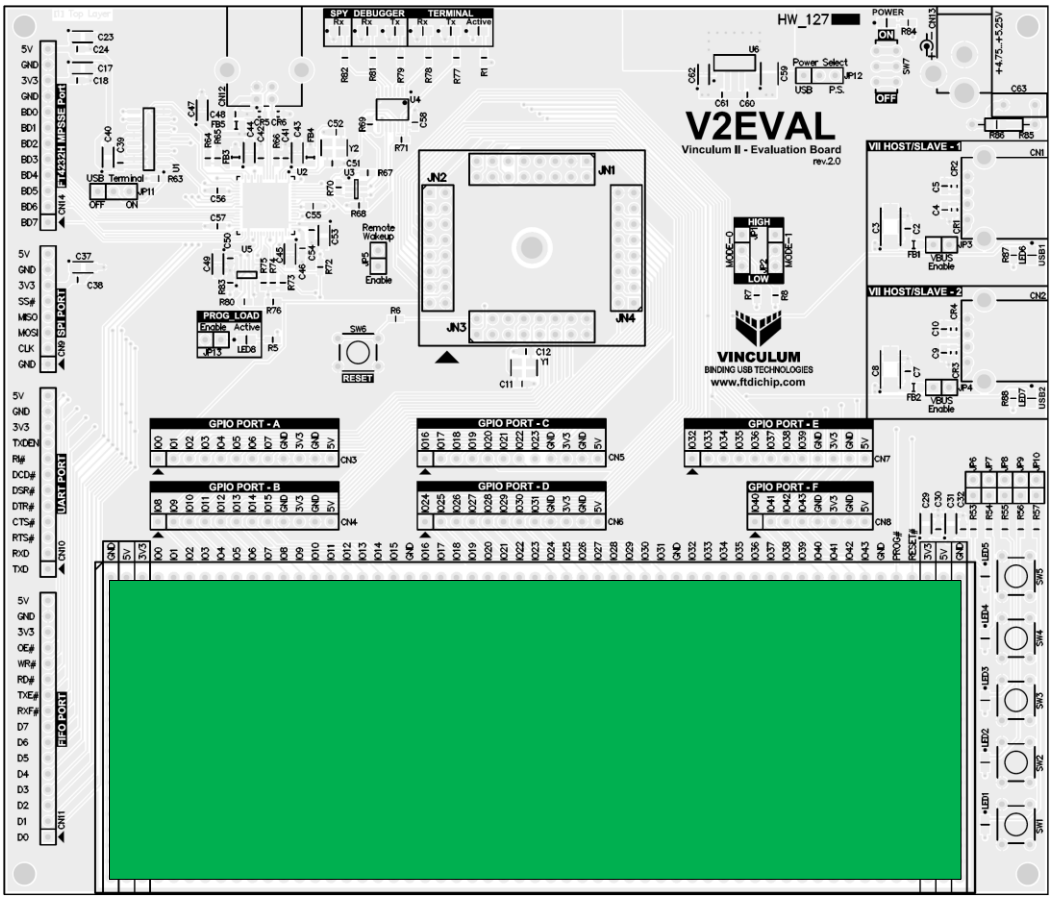


Figure 5.11 : Prototyping area PA1

A prototype area consisting of an array of 1100, 0.1-inch pitch holes is provided. The area can be used to create custom circuitry and connect components to the V2-EVAL board. The prototyping area includes connections to the 5V, 3.3 V planes and ground planes. The silk-screen text on the board indicates which holes are connected to which signals. Only the first column is connected to VNC2 IO ports, power and ground planes. All the other holes are not connected to anything on the board.

Signal pins are shared between other IO connectors on the board. For more information refer to the V2-Eval Board schematics.

Connector pin number	Silk Screen Signal Label	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
1	GND	-	-	-	-	Ground pin
2	5V [32]	-	-	-	-	5V power rail. Can be used to power external devices
3	3V3[33]	-	-	-	-	3.3V power rail. Can be used to power external devices
4	IO0[34]	11	11	11	IO	IOBUS port Data Bit 0. Debug port – default configuration.
5	IO1[34]	12	12	12	IO	IOBUS port Data Bit 1.
6	IO2[34]	14	13	13	IO	IOBUS port Data Bit 2.
7	IO3[34]	15	14	14	IO	IOBUS port Data Bit 3.
8	IO4[34]	-	-	15	IO	IOBUS port Data Bit 4.
9	IO5[34]	-	-	16	IO	IOBUS port Data Bit 5.
10	IO6[34]	-	-	17	IO	IOBUS port Data Bit 6.
11	IO7[34]	-	-	18	IO	IOBUS port Data Bit 7.
12	IO8[34]	-	-	19	IO	IOBUS port Data Bit 8.
13	IO9[34]	-	-	20	IO	IOBUS port Data Bit 9.
14	IO10[34]	-	-	22	IO	IOBUS port Data Bit 10.
15	IO11[34]	-	-	23	IO	IOBUS port Data Bit 11.
16	IO12[34]	-	-	24	IO	IOBUS port Data Bit 12.
17	IO13[34]	-	-	25	IO	IOBUS port Data Bit 13.
18	IO14[34]	-	-	26	IO	IOBUS port Data Bit 14.
19	IO15[34]	-	-	27	IO	IOBUS port Data Bit 15.
20	GND	-	-	-	-	Ground pin
21	IO16[34]	-	-	27	IO	IOBUS port Data Bit 16.
22	IO17[34]	-	46	28	IO	IOBUS port Data Bit 17.
23	IO18[34]	-	45	29	IO	IOBUS port Data Bit 18.
24	IO19[34]	-	48	31	IO	IOBUS port Data Bit 19.
25	IO20[34]	23	31	32	IO	IOBUS port Data Bit 20.
26	IO21[34]	24[35]	32[35]	39	IO	IOBUS port Data Bit 21.
27	IO22[34]	25	33	40	IO	IOBUS port Data Bit 22.
28	IO23[34]	26[35]	34[35]	41	IO	IOBUS port Data Bit 23.
29	IO24[34]	-	35	43	IO	IOBUS port Data Bit 24.
30	IO25[34]	-	36	44	IO	IOBUS port Data Bit 25.
31	IO26[34]	-	37	45	IO	IOBUS port Data Bit 26.
32	IO27[34]	-	38	46	IO	IOBUS port Data Bit 27.
33	IO28[34]	-	41	47	IO	IOBUS port Data Bit 28.
34	IO29[34]	-	42	48	IO	IOBUS port Data Bit 29.
35	IO30[34]	-	43	49	IO	IOBUS port Data Bit 30.
36	IO31[34]	-	44	50	IO	IOBUS port Data Bit 31.
37	GND	-	-	-	-	Ground pin
38	IO32[34]	29	15	51	IO	IOBUS port Data Bit 32.
39	IO33[34]	30	16	52	IO	IOBUS port Data Bit 33.
40	IO34[34]	31	18	55	IO	IOBUS port Data Bit 34.
41	IO35[34]	32	19	56	IO	IOBUS port Data Bit 35.

42	IO36(34)	-	-	57	IO	IOBUS port Data Bit 36.
43	IO37(34)	-	-	58	IO	IOBUS port Data Bit 37.
44	IO38(34)	-	-	59	IO	IOBUS port Data Bit 38.
45	IO39(34)	-	-	60	IO	IOBUS port Data Bit 39.
46	IO40(34)	-	20	61	IO	IOBUS port Data Bit 40.
47	IO41(34)	-	21	62	IO	IOBUS port Data Bit 41.
48	IO42(35)	-	22	63	-	IOBUS port Data Bit 42.
49	IO43(35)	-	23	64	-	IOBUS port Data Bit 43.
50	GND	-	-	-	-	Ground pin
51	PROG#	9	10	10	I	VNC2 PROG# pin
52	RESET#	10	9	9	I	VNC2 RESET# pin
53	3V3(33)	-	-	-	-	3.3V power rail. Can be used to power external devices
54	5V(32)	-	-	-	-	5V power rail. Can be used to power external devices
55	GND	-	-	-	-	Ground pin

Notes:

(32) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

(33) This pin is connected to 3.3V regulator output.

(34) The IOBUS signal labels on the PCB silk screen do directly relate to the IOBUS signal names for the VNC2 device on the daughterboard. See VNC2 pin number for signal mapping on the device.

(35) The following pins are only accessible when the onboard multiplexer select input is high. See section 6.4 for details.

Table 5.10 : Prototyping Area Pinout

5.7 USB1 interface CN1

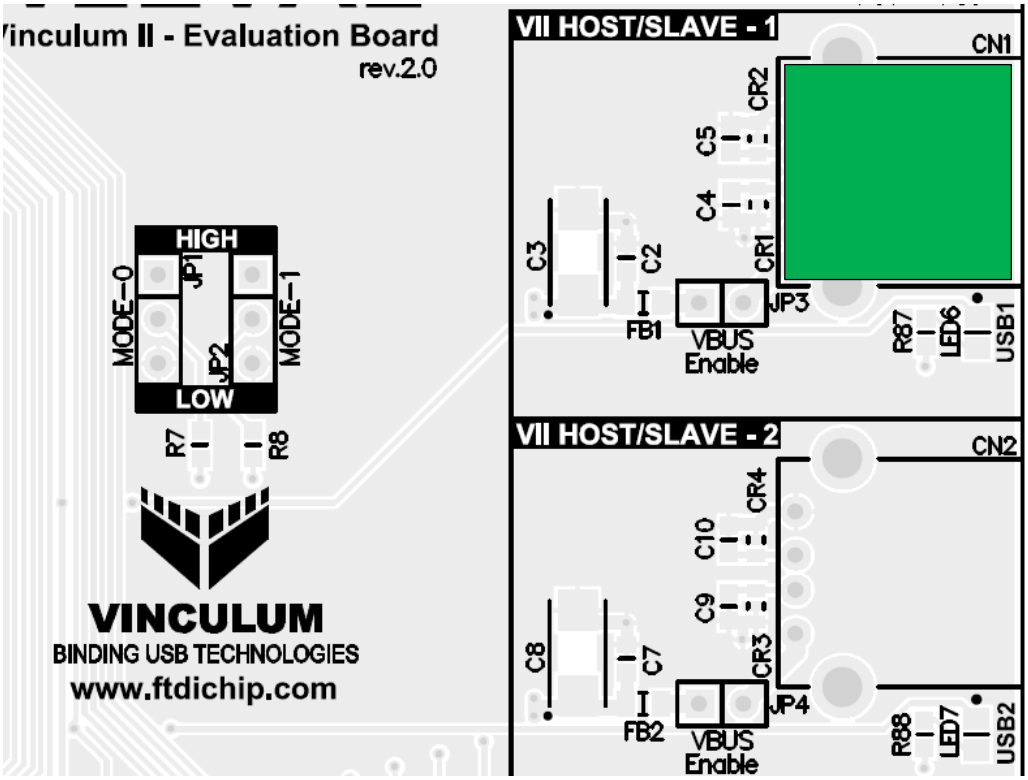


Figure 5.12 : USB1 Interface CN1

VNC2 USB1 transceiver pins are brought on this connector. Depending on the firmware version this port can be configured as host or slave port.

Signal name	Connector pin number	VCN2 pin name	VCN2 pin number			IO type	Description
			32-PIN	48-PIN	64-PIN		
5V (36)	1	-	-			-	5V power rail. Can be used to power external devices
USB1-DM	2	USB1 DM	18	26	34	IO	USB1 transceiver, data line Minus
USB1-DP	3	USB1 DP	17	25	33	IO	USB1 transceiver, data line Plus
GND	4	-	-			-	Ground pin
Shield	5, 6	-	-			-	Connector shield. Connected to ground.

Notes:
(36) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

Table 5.11 : USB1 Host/Slave Connector CN1

5.8 USB2 interface CN2.

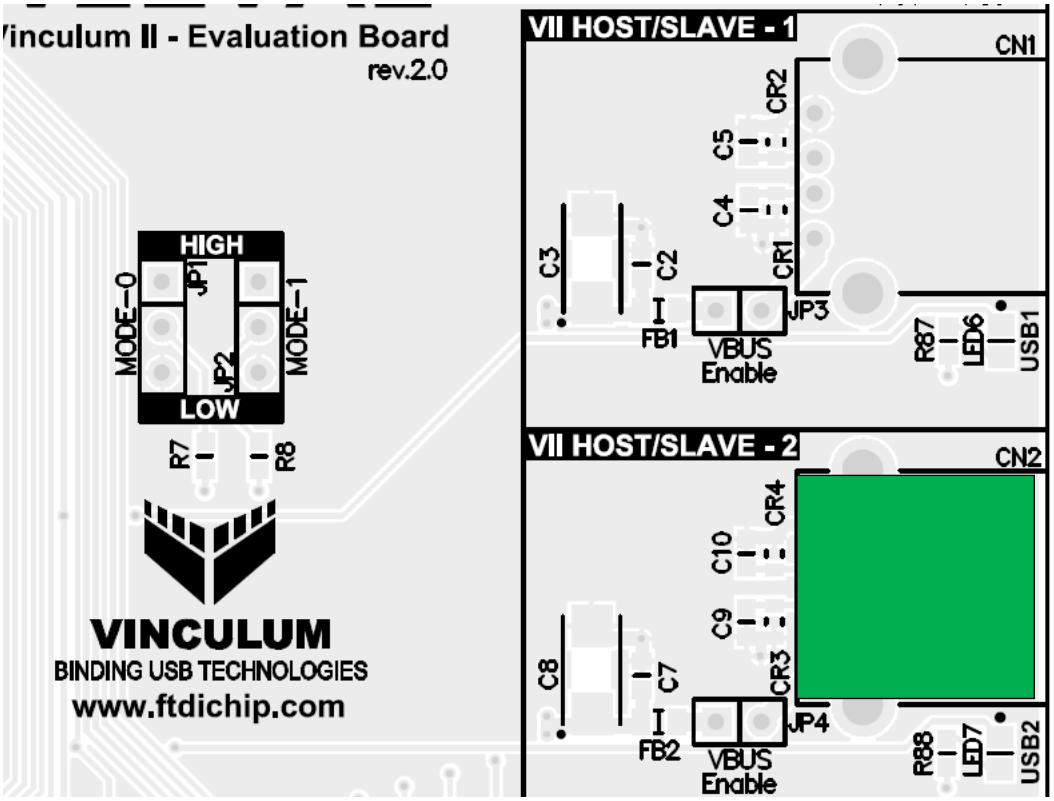


Figure 5.13 : USB2 Interface CN2

VNC2 USB2 transceiver pins are brought on this connector. Depending on the version of the firmware running on the device, the port can be configured as host or slave port.

Signal name	Connector pin number	VCN2 pin name	VCN2 pin number			IO type	Description
			32-PIN	48-PIN	64-PIN		
5V (37)	1	-	-			-	5V power rail. Can be used to power external devices
USB2-DM	2	USB2 DM	21	29	37	IO	USB2 transceiver, data line Minus
USB2-DP	3	USB2 DP	20	28	36	IO	USB2 transceiver, data line Plus
GND	4	-	-			-	Ground pin
Shield	5, 6	-	-			-	Connector shield. Connected to ground.

Notes:
(37) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

Table 5.12 : USB2 Host / Slave connector CN2

5.9 VNC1L Interface Mode Select / GPIO Jumpers JP1, JP2

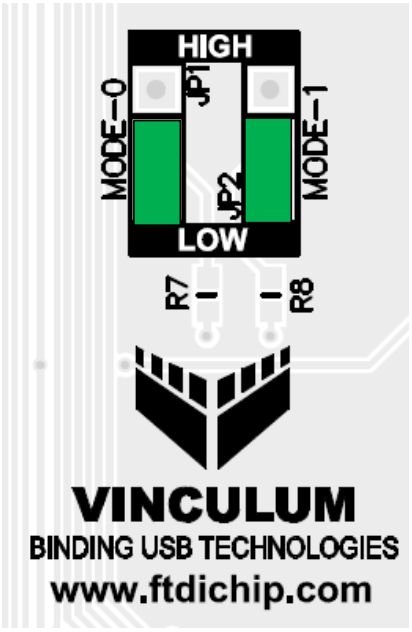


Figure 5.14 : GPIO Jumper pins, JP1, JP2

JP1 and JP2 jumpers are designed to provide backwards compatibility for VNC1L firmwares migrated to the VNC2. The jumpers are used select between the UART, FIFO and SPI slave interface for use as the monitor port on the VNC1L. The jumper configurations for each interface are listed in Table 5.14. More details on the monitor port are available in the VNC1L Firmware User Manual (FT_000006).

When not running VNC1L firmwares, jumpers JP1 and JP2 can be used by designers as general purpose GPIO jumper select inputs to the VNC2.

Jumper	VNC2 Pin Number / Signal Name		VNC2 Signal Name Comments
	48-PIN	64-PIN	
JP1	46 / IOBUS25(38)	29 / IOBUS17	INT_SEL0. Signal also connected to LED5
JP2	47 / IOBUS26	-	INT_SEL1.

Notes:

(38) To run VNC1L firmwares, jumper JP9 must also be removed.

(39) The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

Table 5.13 : GPIO jumpers JP1, JP2

JP1 (INT_SEL0)	JP2 (INT_SEL1)	Mode
Pull-up	Pull-up	Serial UART
Pull-down	Pull-up	SPI
Pull-up	Pull-down	FIFO
Pull-down	Pull-down	Serial UART

Table 5.14 : Monitor Interface Select – VNC1L Firmware Backwards Compatiblity

5.10 User LEDs. LED1 – LED5.

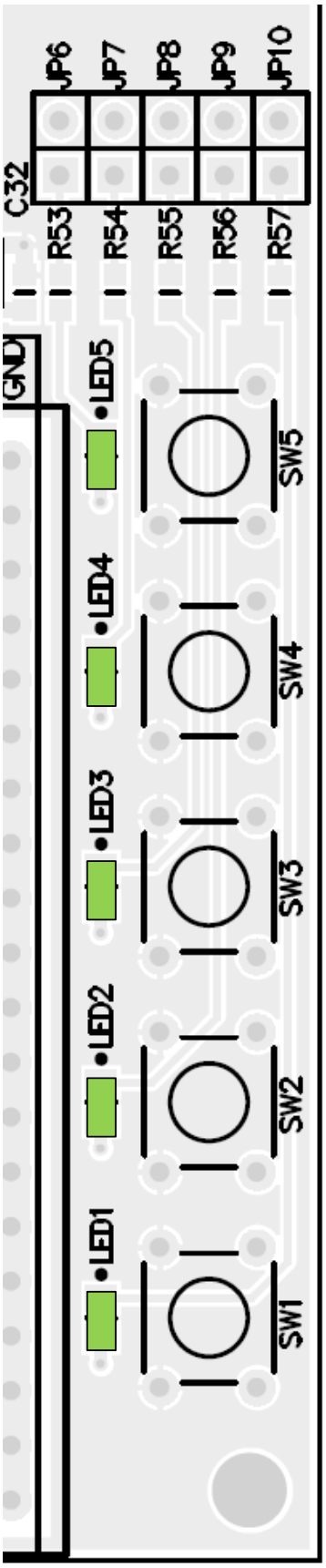


Figure 5.15 : User LEDs

Five LEDs are provided on board. The LEDs enabled or disabled via jumpers JP6 – JP10. The LEDs are controlled by the IOBUS signals on the VNC2.

Designator	VCN2 pin number		
	32-PIN	48-PIN	64-PIN
LED1	32	19	56
LED3	-	20	61
LED4	-	21	62
LED5	-	22	64
LED6	-	23	64
Notes:			

Table 5.15 : User LED connections

5.11 LED enable/disable jumpers JP6 – JP10.

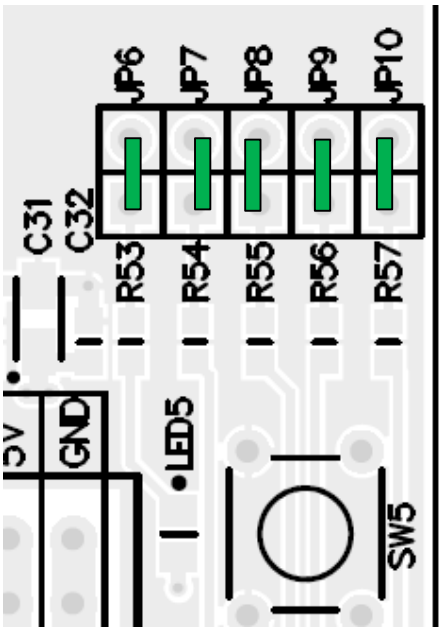


Figure 5.16 : LED Enable/Disable jumpers

Every user-defined LED have an enable/disable jumper. When jumper is closed LED will be illuminate when driven low by one of the VNC2 pins. When jumper is opened LED is disconnected from the VCN2 pin.

Designator	LED affected
JP6	LED5
JP7	LED4
JP8	LED3
JP9	LED2
JP10	LED1
Notes:	

Table 5.16 : LED Enable/Disable Jumpers.

5.12 User push button switches

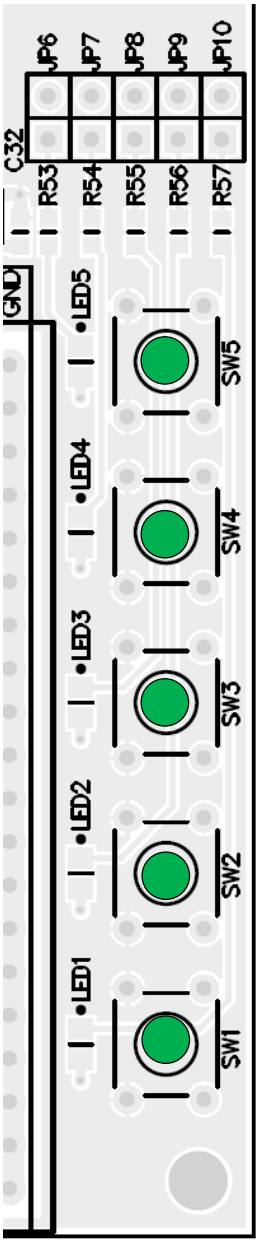


Figure 5.17 : User Push Button Switches

Push button switches connected straight to VNC2 pins. When the switch is pressed down, a logic LOW appears on the corresponding VNC2 pin.

Designator	VNC2 Pin Number		
	32-PIN	48-PIN	64-PIN
SW1(40)	12	12	12
SW2(40)	14	13	13
SW3(40)	15	14	14
SW4(40)	29	15	51
SW5(40)	-	48	32

Notes:

(40) The IOBUS pins are shared by other connectors on the board. Care should be taken to ensure that operation of the switches does not interfere with pins used by other headers on the board. Also it is advisable to always set the pull-up resistor in the IO cell configuration for the specified pin (i.e. `pull` setting of `vos_iocell_set_config` should be set to `VOS_IOCELL_PULL_UP_75K`).

Table 5.17 User Switches

5.13 Host USB power jumpers JP3, JP4.

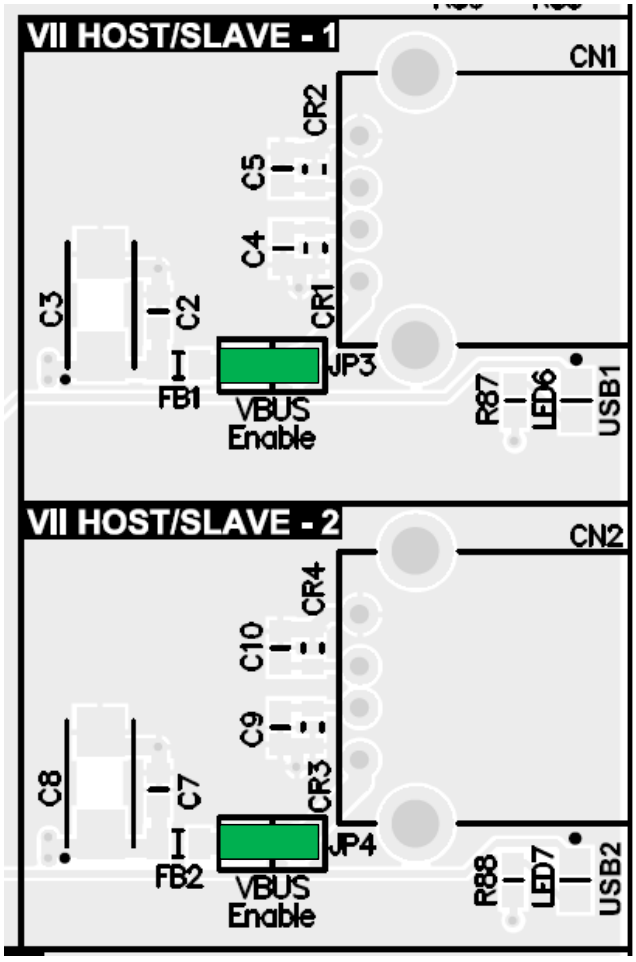


Figure 5.18 : USB Power Enable Jumpers JP4 and JP5

When either USB1 and/or USB2 ports are used as a host ports, the jumpers JP3 and/or JP4 accordingly should be closed to allow peripheral devices to draw power from board's +5V power rail.

Warning!

When using USB1 and USB2 ports as a USB slave ports, remove the shunts from jumpers JP3 and JP4. Failure to do so could cause damage to the USB host or to the V2-EVAL board.

5.14 Remote Wakeup jumper JP5.

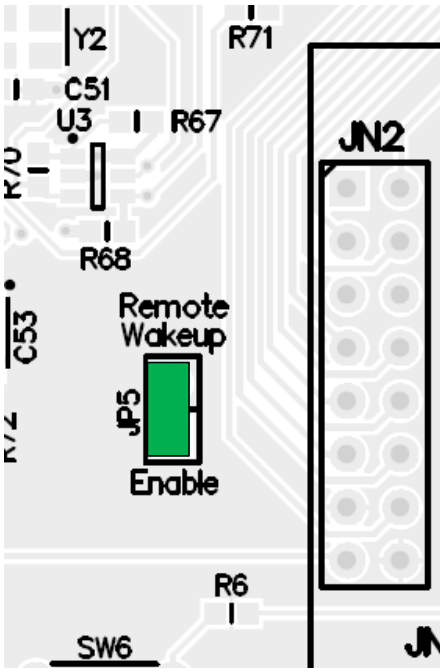


Figure 5.19 : Remote Wakeup Jumper

The remote wakeup jumper enables any firmware running on the VNC2 to support Suspend Monitor (SUM) mode, allowing the device to reduce power consumption when idle. The VNC2 device can be configured to wakeup when any data arrives on the receive data (RXD) pin, by connecting the RXD pin to ring indicator (RI#) input via jumper JP5. When RI# pin is driven low, VNC2 will resume from the SUM mode immediately. The remote wakeup feature is only available when using the UART interface on the VNC2. The feature can be enabled when a jumper is present on jumper JP5.

5.15 Reset Push-button Switch

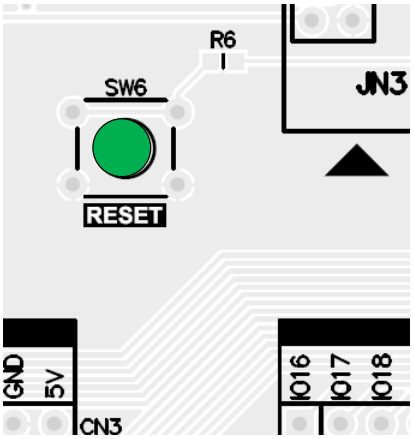


Figure 5.20 : Reset Switch

A 'RESET' push button switch is provided on switch SW6, to enable manual resetting of the VNC2 device.

5.16 'PROG' LED

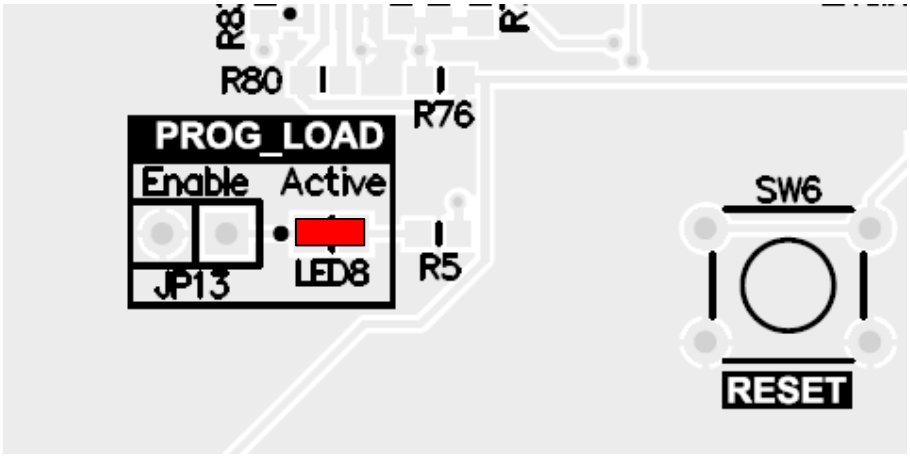


Figure 5.21 : 'PROG' LED

LED8 (red) is provided to indicate when VNC2 device is in Flash programming mode.

5.17 VNC2 Daughterboard Connector – JN1

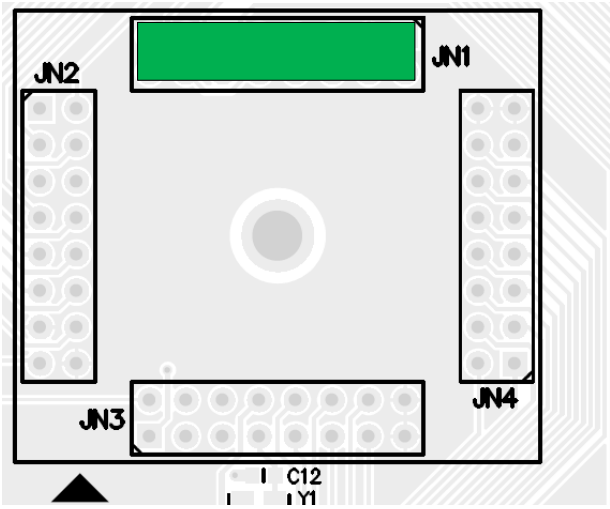


Figure 5.22 : VNC2 Daughterboard Connector JN1

Schematic Signal Name[41]	Connector Pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
3V3	1	-	-	-	-	3.3V power rail.
3V3	2	-	-	-	-	3.3V power rail.
GND	3	-	-	-	-	Ground pin.
DP1	4	17	25	33	IO	USB1 transceiver, data line positive connected to CN1.
DM1	5	18	26	34	IO	USB1 transceiver, data line minus connected to CN1.
IO32	6	29	15	51	IO	Connected to PA1 pin 38 / CN7 pin 1 / CN11 pin 13.
IO33	7	30	16	52	IO	Connected to PA1 pin 39 / CN7 pin 2.
IO34	8	31	18	55	IO	Connected to PA1 pin 40 / CN7 pin 3.
IO35	9	32	19	56	IO	Connected to PA1 pin 41 / CN7 pin 4.
DP2	10	20	28	36	IO	USB2 transceiver, data line positive connected to CN2.
DM2	11	21	29	37	IO	USB2 transceiver, data line minus connected to CN2.
IO20	12	23	31	39	IO	Connected to PA1 pin 25 / CN5 pin 5 / CN9 pin 2 / CN10 pin 1 / CN11 pin 1.
VIO21	13	24	32	40	IO	Connected to U1 channel 3 output
IO22	14	25	33	41	IO	Connected to PA1 pin 27 / CN5 pin 7 / CN10 pin 3 / CN9 pin 4 / CN11 pin 3.
VIO23	15	26	34	42	IO	Connected to U1 channel 2 output
IO24	16	-	35	43	IO	Connected to PA1 pin 29 / CN6 pin 1 / CN10 pin 5 / CN11 pin 5.

Notes:
(41) The signal names relate to the labels used on pages 1 & 2 of the V2-EVAL base board schematic. Unless otherwise stated, the function of the IO signals is be set by the user application running on the VNC2.

Table 5.18 : Connector JN1 Pinout

5.18 VNC2 Daughterboard Connector – JN2

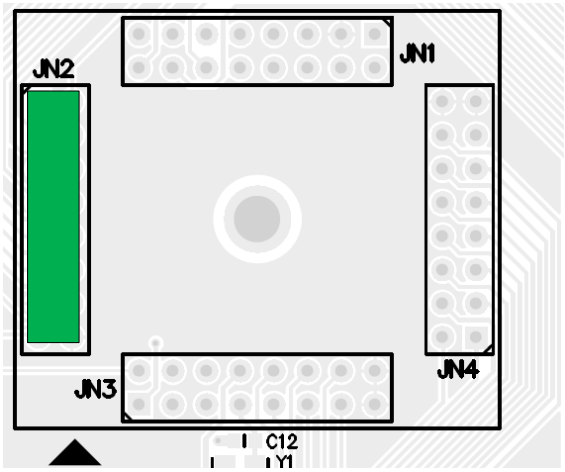


Figure 5.23 : VNC2 Daughterboard Connector JN2

Schematic Signal Name[42]	Connector Pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
VIO25	1	-	36	44	IO	Connected to U1 channel 1 output
IO26	2	-	37	45	IO	Connected to PA1 pin 31 / CN6 pin 3 / CN10 pin 7 / CN11 pin 7.
IO27	3	-	38	46	IO	Connected to PA1 pin 32 / CN6 pin 4 / CN10 pin 8 / CN11 pin 8.
IO28	4	-	41	47	IO	Connected to PA1 pin 33 / CN6 pin 5 / CN10 pin 9 / CN11 pin 9.
3.3V	5	-	-	-	-	3.3V power rail.
3.3V	6	-	-	-	-	3.3V power rail.
IO29	7	-	42	48	IO	Connected to PA1 pin 34 / CN6 pin 6 / CN11 pin 10.
IO30	8	-	43	49	IO	Connected to PA1 pin 35 / CN6 pin 7 / CN11 pin 11.
IO31	9	-	44	50	IO	Connected to PA1 pin 36 / CN6 pin 8 / CN11 pin 12.
IO36	10	-	-	57	IO	Connected to PA1 pin 42 / CN7 pin 5.
IO37	11	-	-	58	IO	Connected to PA1 pin 43 / CN7 pin 6.
IO38	12	-	-	59	IO	Connected to PA1 pin 44 / CN7 pin 7.
GND	13	-	-	-	-	Ground pin.
IO39	14	-	-	60	IO	Connected to PA1 pin 45 / CN7 pin 8.
IO0	15	11	11	11	IO	Debug pin. Connected to PA1 pin 4 / CN3 pin 1.
GND	16	-	-	-	-	Ground pin.

Notes:
(42) The signal names relate to the labels used on pages 1 & 2 of the V2-EVAL base board schematic. Unless otherwise stated, the function of the IO signals is set by the user application running on the VNC2.

Table 5.19 : Connector JN2 Pinout

5.19 VNC2 Daughterboard Connector – JN3

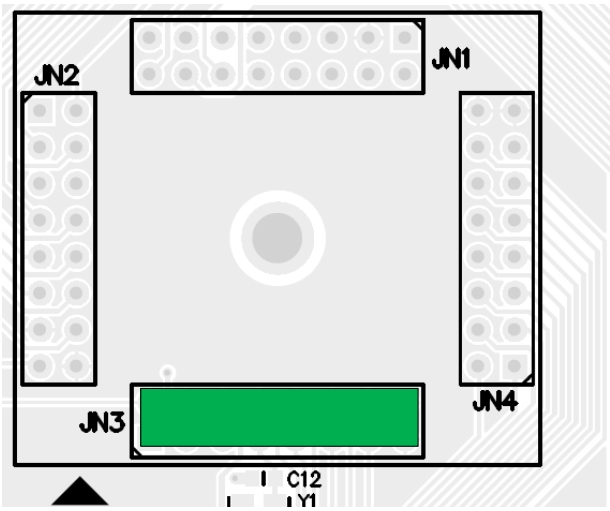


Figure 5.24 : VNC2 Daughterboard Connector JN3

Schematic Signal Name[43]	Connector Pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
PROG#	1	9	10	10	Input	PROG# input to VNC2.
RESET#	2	10	9	9	Input	RESET# input to VNC2.
IO43	3	-	23	64	IO	Connected to PA1 pin 49 / CN8 pin 4.
IO42	4	-	22	63	IO	Connected to PA1 pin 48 / CN8 pin 3.
IO41	5	-	21	62	IO	Connected to PA1 pin 47 / CN8 pin 2.
IO40	6	-	20	61	IO	Connected to PA1 pin 46 / CN8 pin 1.
XTOUT	7	5	5	5	Output	Output from 12MHz oscillator cell on VNC2.
XTIN	8	4	4	4	Input	Input to 12MHz oscillator cell on VNC2.
IO2	9	14	13	13	IO	Connected to PA1 pin 6 / CN3 pin 3.
IO1	10	12	12	12	IO	Connected to PA1 pin 5 / CN3 pin 2.
IO4	11	-	-	15	IO	Connected to PA1 pin 8/CN3 pin 5.
IO3	12	15	14	14	IO	Connected to PA1 pin 7 / CN3 pin 4.
IO6	13	-	-	17	IO	Connected to PA1 pin 10/CN3 pin 7.
IO5	14	-	-	16	IO	Connected to PA1 pin 9/CN3 pin 6.
GND	15	-	-	-	-	Ground pin.
GND	16	-	-	-	-	Ground pin.

Notes:
(43) The signal names relate to the labels used on pages 1 & 2 of the V2-EVAL base board schematic. Unless otherwise stated, the function of the IO signals is set by the user application running on the VNC2.

Table 5.20 : Connector JN3 Pinout

5.20 VNC2 Daughterboard Connector – JN4

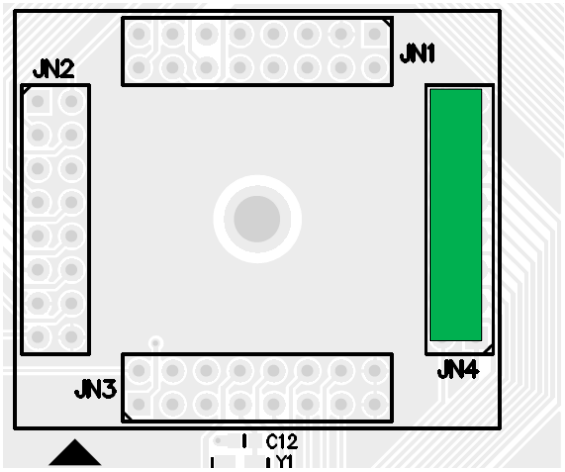


Figure 5.25 : VNC2 Daughterboard Connector JN4

Schematic Signal Name(44)	Connector Pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
IO8	1	-	-	19	IO	Connected to PA1 pin 12 / CN4 pin 1.
IO7	2	-	-	18	IO	Connected to PA1 pin 11 / CN3 pin 8.
IO10	3	-	-	22	IO	Connected to PA1 pin 14 / CN4 pin 3.
IO9	4	-	-	20	IO	Connected to PA1 pin 13 / CN4 pin 2.
IO12	5	-	-	24	IO	Connected to PA1 pin 16 / CN4 pin 5.
IO11	6	-	-	23	IO	Connected to PA1 pin 15 / CN4 pin 4.
IO14	7	-	-	26	IO	Connected to PA1 pin 18 / CN4 pin 7.
IO13	8	-	-	25	IO	Connected to PA1 pin 17 / CN4 pin 6.
IO16	9	-	-	28	IO	Connected to PA1 pin 21 / CN5 pin 1.
IO15	10	-	-	27	IO	Connected to PA1 pin 19 /CN4 pin 8.
IO18	11	-	45	31	IO	Connected to PA1 pin 23 / CN5 pin 3.
IO17	12	-	46	29	IO	Connected to PA1 pin 22 / CN5 pin 2.
MODE1	13	-	47	-	IO	Connected to jumper JP2.
IO19	14	-	48	32	IO	Connected to PA1 pin 24 / CN5 pin 4.
GND	15	-	-	-	-	-
GND	16	-	-	-	-	-

Notes:
(44) The signal names relate to the labels used on pages 1 & 2 of the V2-EVAL base board schematic. Unless otherwise stated, the function of the IO signals is set by the user application running on the VNC2.

Table 5.21 : Connector JN4 Pinout

5.21 FT4232H MPSSE Connection – CN14

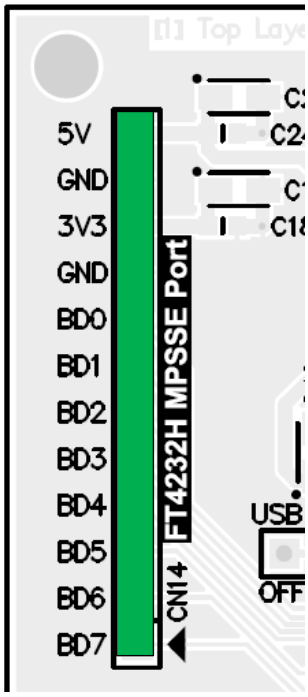


Figure 5.26 : CN14 – FT4232H MPSSE port

Schematic Signal Name	Connector Pin	Description
BD7	1	FT4232H channel B BDBUS7
BD6	2	FT4232H channel B BDBUS6
BD5	3	FT4232H channel B BDBUS5
BD4	4	FT4232H channel B BDBUS4
BD3	5	FT4232H channel B BDBUS3
BD2	6	FT4232H channel B BDBUS2
BD1	7	FT4232H channel B BDBUS1
BD0	8	FT4232H channel B BDBUS0
GND	9	Ground pin.
3V3	10	3.3V power rail.
GND	11	Ground pin.
5V	12	5V power rail.

Table 5.22 : Connector CN14 Pinout

MPSSE – Multi Purpose Synchronous Serial Engine allows the FT4232H to master any synchronous serial interface e.g. I2C, SPI or JTAG. For more information see: AN135 – MPSSE Basics (http://www.ftdichip.com/Support/Documents/AppNotes/AN_135_MPSSE_Basics.pdf)

6 FT4232H Configuration

The V2-EVAL board features a FT4232H, a high speed USB to quad channel UART / serial converter device. The device is primarily featured to provide a connection from the board to a PC host via the onboard USB type B connector. Each of the four channels on the FT4232H device are used to provide a separate functions on the V2-EVAL board.

The functions of the FT4232H include:

- Channel A – UART interface. The FT4232H provides USB to UART conversion to allow a PC / USB host PC to communicate with the VNC2, via the UART interface.
- Channel B – MPSSE data port for JTAG, I2C or SPI communication via connector CN14 on the board.
- Channel D - Provide a UART data 'sniffer' interface allowing inputs to the VNC2 UART interface to be displayed on the host PC software.
- Channel D – Device control. I/O pins are used to control the onboard multiplexer. The multiplexer allows different interfaces to drive the VNC2 UART interface as well as the VNC2 PROG# and RESET# pins.

Figure 6.1, outlines the configuration circuit for FT4232H I/O ports.

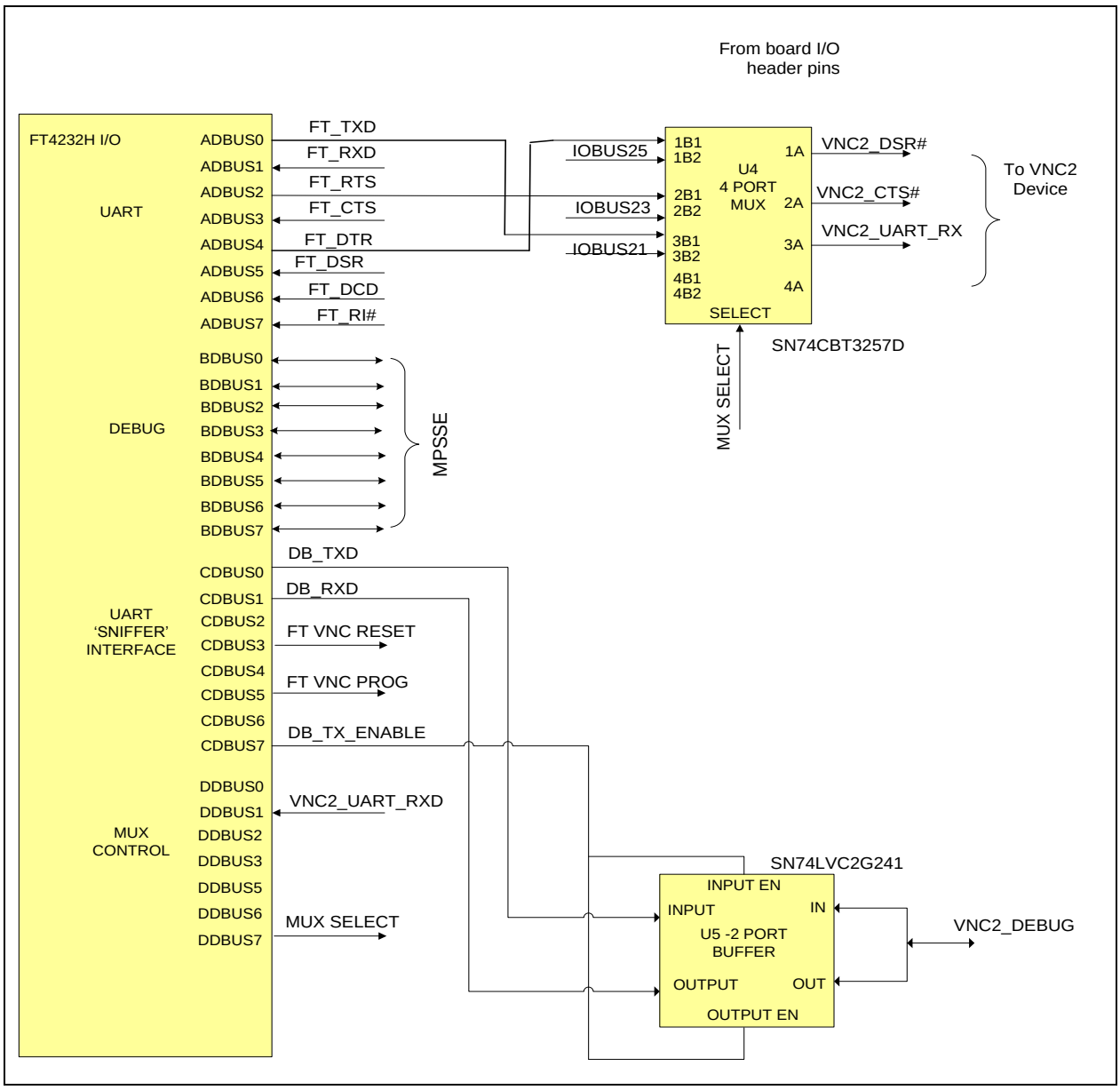


Figure 6.1 : FT4232H Configuration

6.1 UART Interface

The FT4232H channel A, ADBUS I/O, pins are used for UART operation with the VNC2. The UART inputs to the FT4232H are supplied directly from the VNC2 device pins, while the UART outputs from the FT4232H, are passed to an external multiplexer. The multiplexer allows the UART interface to the VNC2 to be driven by either by the FT4232H device or by an external UART device, which is connected to the V2-EVAL board via the various board I/O header pins. The multiplexer select pin is controlled by pin DDBUS0 on the FT4232H, where a logic '0' on the select pin will force the FT4232H device to drive the UART interface on the VNC2, while a logic '1' will allow IOBUS21 and IOBUS23 header pins on the board to drive the UART.

6.2 Debug Interface – UART Mode

The FT4232H channel C I/O pins are used to control the debug interface on the VNC2 device. The channel is used to allow the device debug pin to be connected to a software debugger environment running on a PC. The single bit, bi-directional debug signal from VNC2 is converted into a UART style interface, with separate transmit and receive signals via a 2-port buffer. The signal on the CDBUS0 pin corresponds to the transmit data from the debug software, while CDBUS1 corresponds to the receive output from the VNC2. Pin CDBUS7, DBGTXEN, on the FT4232H is used for controlling transmit and receive operation on the 2 port buffer. When signal DBGTXEN is '0' then the signal IO0 (debug pin of VNC2) will drive the DBGRX input to the FT4232H. Alternatively when DBGTXEN is '1' then the FT4232H UART output DBGTX will drive the VNC2_DEBUG signal (IO0).

6.3 UART 'Spy' Interface

Channel D on the FT4232H device is configured as a UART interface. The channel is used as a 'data spy' to detect any data sent to the VNC2 UART interface. The detected data is passed to software running on the PC for display. The feature is used for detecting and displaying UART data from external sources which are connected to the VNC2 UART interface, via the board I/O headers.

6.4 Device Control – Bit Bang Mode

The I/O signals on FT4232H channel C are used for additional control functions on the board. Pins CDBUS3 and CDBUS5 are used for controlling the RESET# and PROG# inputs on the VNC2 from the software via the FT4232H in bit bang mode.

Pin DDBUS7 on the FT4232H channel D is used to control the channel select input on the multiplexer. A logic '0' on the multiplexer select pin will force multiplexer input B1 to drive the multiplexer output A, while a logic '1' will force multiplexer input B2 to drive the multiplexer output.

Table 6.1, summarises the V2-EVAL board settings based on the value of the multiplexer select pin.

Multiplexer Select Pin Status (Set by FT4232H DDBUS7)	Board Configuration Status
0	VNC2 UART interface connected to FT4232H channel A.
1	VNC2 UART interface connected to header pins on V2-EVAL board.

Table 6.1 : Multiplexer Configuration Settings

7 Connecting to a PC Host

Connect a USB A/B cable to USB slave connector CN12 on the V2-EVAL board. Connect the other end to PC computer and power-up the board. The PC should detect that new hardware has been plugged into the PC and will launch the Hardware Wizard for installing the drivers. The driver installation procedure is outlined in the following section.

7.1 Driver Installation

The FTDI USB drivers are required for the USB slave interface to FT4232H on the V2-EVAL board. The latest drivers can be downloaded from the FTDI website http://www.ftdichip.com/Drivers/VCP.htm.

Installation instructions detailing all the steps required to install drivers on different operating systems are available from http://www.ftdichip.com/Documents/InstallGuides.htm. A summary of the installation steps for a Windows XP system are shown below.

Upon connection, the New Hardware Wizard should produce the following screen shown in

1. Figure 7.1.

   As FTDI supply WHQL certified drivers a user may select the option 'Yes, this time only', which will cause the Hardware Wizard to download compatible FTDI drivers from the internet. However to avoid internet connectivity issues, users may carry out a manual installation using the following steps.

Figure 7.1 : Found New Hardware Wizard Screen

2. With the manual installation, select the option to "Install from a list or specific location (Advanced)" as shown in Figure 7.2 below and then click "Next".

Figure 7.2 : Select installation option

3. Select "Search for the best driver in these locations" and enter the file path in the combo-box ("C:\ CDM 2.06.00 WHQL Certified\CDM 2.06.00 WHQL Certified" in Figure 7.3 below) or browse to it by clicking the browse button. Once the file path has been entered in the box, click next to proceed.

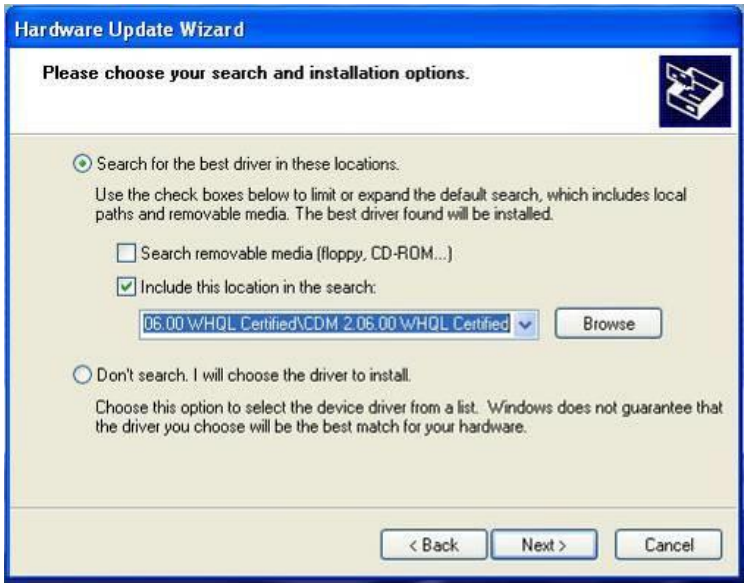


Figure 7.3 : Select location of the driver

If installing a non-WHQL certified driver, then users may receive a warning, similar to Figure 7.4, stating that the driver has not passed Windows Logo testing. If the warning is received, click on 'Continue Anyway' to continue with the installation.

Figure 7.4 : Non-WHQL Driver Warning

Note: If a later driver version exists we recommend using that.

4. In the next screen the Hardware Wizard will copy the the required driver files.

Figure 7.5 : Driver installation

5. In the next stage, the process will repeat another three times until all four ports on the FT4232H have been identified by the operating system. Windows should present a message to inform whether or not the drivers for each port have been successfully installed.

6. To verify that the drivers have been installed successfully, open the Device Manager located in "Control Panel\System" then select the "Hardware" tab and click "Device Manger") and select "View > Devices by Connection". Each FT4232H port should appear as a "USB Serial Converter" under the "USB Serial Bus Controllers". Further under the "Ports" section four "USB Serial Ports" should be listed, as per Figure 7.6.

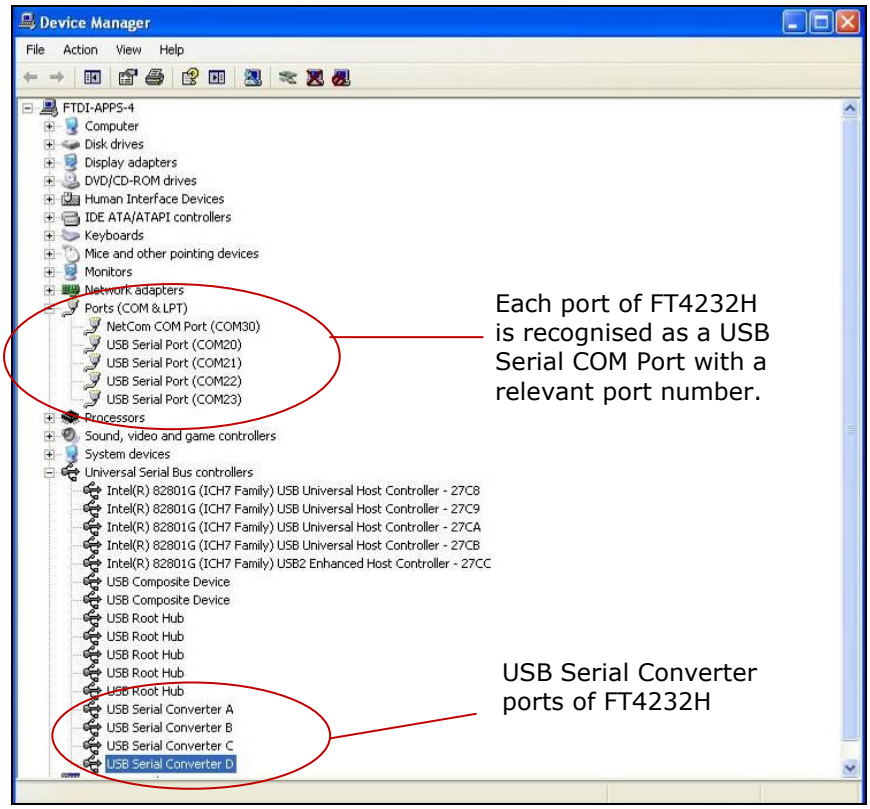


Figure 7.6 : Device Manager Screen

8 V2-EVAL Software

The following section details instructions on how to install and use the V2-EVAL software terminal utility for the V2-EVAL board.

8.1 V2-EVAL Terminal Installation

A simple terminal application has been designed for use with the VNC2 V2-EVAL board. The application can be downloaded as part of the Vinculum II utilities available from:

http://www.ftdichip.com/Firmware/VNC2tools.htm

Note:

The V2-EVAL terminal software is only supported under WindowXP, Vista and Windows 7 Operating Systems.

To install the terminal application, simply double click on the installer and follow the installation instructions shown.

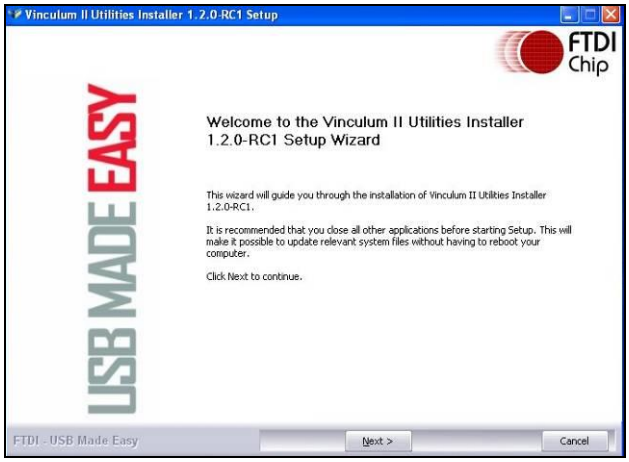


Figure 8.1 : Installer Introduction Screen

Once installation is complete, the V2-EVAL application can be found and launched from 'Start -> 'All Programs -> FTDI -> Vinculum II Utilities' location.

8.2 Using V2-EVAL Terminal

The V2-EVAL terminal utility is a standard terminal application designed specifically to support the V2-EVAL board. The application provides communication to the UART interface on the VNC2 device and also provides commands to control some basic configuration functions on the V2-EVAL board. All communication and control commands are directed to the V2-EVAL board via the onboard FT4232H USB to quad channel serial converter.

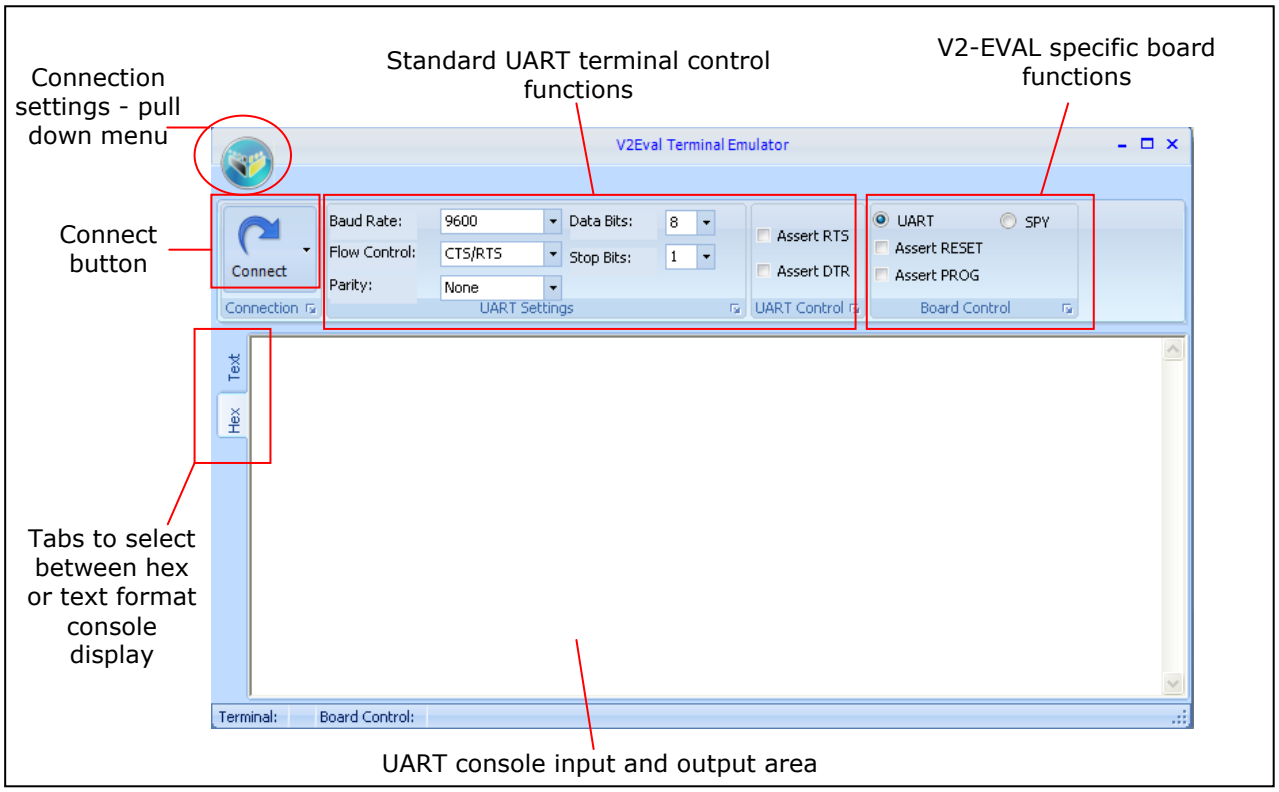


Figure 8.2 : V2-EVAL Terminal Utility Features

The V2-EVAL utility supports standard terminal commands and control functions. Pull down menus list different UART speeds, and data settings. On the top right hand section of the software a set of check buttons are available for controlling the V2-EVAL board. A summary of the function of each button on the V2-EVAL terminal utility is outlined below:

- '**Connect'** button – Connects and disconnects the terminal utility from the UART hardware.
- '**Assert RTS'** checkbox – Assert the Request To Send line on the UART interface.
- **'Asset DTR'** checkbox – Assert Data Terminal Ready line on the UART interface.
- **'UART'** mode button – Enables full UART TX and RX operation through the V2-EVAL terminal utility. Under the UART mode the select line of the V2-EVAL board multiplexer U4 is set to '0' forcing the FT4232H channel A to connect to UART interface on VNC2, as per the conditions outlined in Table 6.1.
- '**Spy'** mode button – The 'Spy' button sets the select line of the V2-EVAL board multiplexer U4 to '1', allowing the VNC2 UART interface to be controlled by an external device connected to the V2-EVAL board instead of the FT4232H, as per the conditions outlined in Table 6.1. Under this setting a user can connect to V2-EVAL board in 'Spy' mode via FT4232H channel C and observe VNC2 UART RX data in the terminal utility. 'Spy' mode is a read-only UART mode. Any user data input to the console under this mode is ignored.
- **'Assert RESET'** checkbox – When checked the software will enable the RESET# input signal on the VNC2 device. The checkbox is only available under UART mode.
- **'Assert PROG'** checkbox - When checked, the software will enable the PROG# input signal on the VNC2 device. The checkbox is only available under UART mode.

8.2.1.1 Using the V2-EVAL Terminal 'Spy' Mode

The V2-EVAL hardware and terminal utility supports a 'Spy' mode enabling the V2-EVAL terminal utility to display data from the VNC2 UART RXD pin, when the VNC2 is communicating with an external UART device. The following section outlines the steps to connect an external UART device to the VNC2 interface and enabling the 'Spy' mode.

1. The first step is to connect an external UART device to the VNC2 UART interface on the V2-EVAL board. An external device can be connected to the board via I/O connectors CN3 – CN11 or via the IOBUS connections in prototyping area PA1.
2. The next step is to configure the IOMUX configuration settings on the VNC2 device to check that the UART connections reflect the physical I/O pins being used on the V2-EVAL hardware. The IOMUX settings are set within the VNC2 software code. A code example showing how to configure the VNC2 IOMUX settings is shown in Figure 8.3.

```
if (vos_get_package_type() == VINCULUM_II_64_PIN)
{
   // UART to V2EVAL board pins
   vos_iomux_define_output(39,IOMUX_OUT_UART_TXD); //UART Tx to pin 39
   vos_iomux_define_input(40,IOMUX_IN_UART_RXD); //UART Rx to pin 40
   vos_iomux_define_output(41,IOMUX_OUT_UART_RTS_N); //UART RTS# to pin 41
   vos_iomux_define_input(42,IOMUX_IN_UART_CTS_N); //UART CTS# to pin 42
}
else // VINCULUM_II_48_PIN
{
    // UART to V2EVAL board pins
    vos_iomux_define_output(31,IOMUX_OUT_UART_TXD); //UART Tx to pin 31
    vos_iomux_define_input(32,IOMUX_IN_UART_RXD); //UART Rx to pin 32
    vos_iomux_define_output(33,IOMUX_OUT_UART_RTS_N);//UART RTS# to pin 33
    vos_iomux_define_input(34,IOMUX_IN_UART_CTS_N); //UART CTS# to pin 34
}
```

Figure 8.3 : Example IOMUX configuration code

The IOMUX configuration code can also be automatically generated using the Vinculum IOMUX configuration utility, which is available as part of the Vinculum II development tools.

The IOMUX settings are incorporated into the VNC2 firmware file as part of the VNC2 software development process. The settings are applied to the VNC2 when the firmware image is downloaded to the VNC2 device.

3. With the VNC2 device now programmed for UART operation, the next stage is to configure the V2-EVAL terminal utility for 'Spy' mode. Open the utility and connect to the board. In the 'Board Control' panel select the 'Spy' button. The step will reconfigure the onboard multiplexer. After changing to 'Spy' mode disconnect the terminal connection.

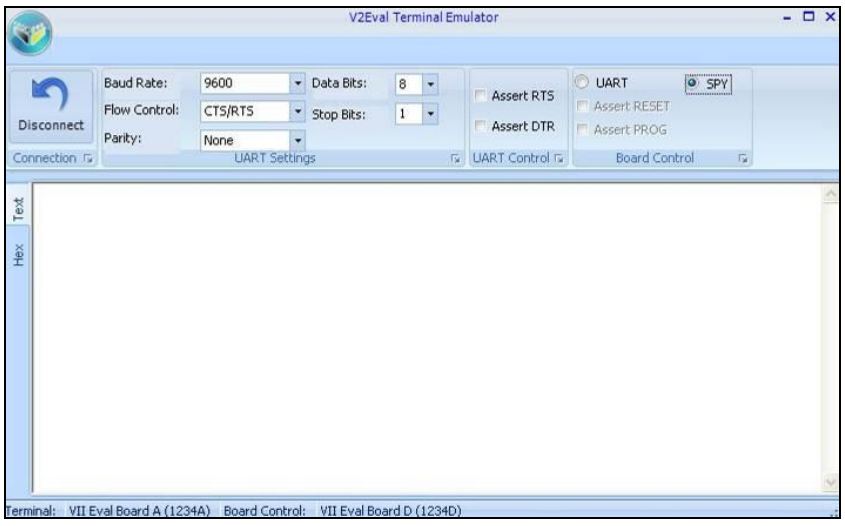


Figure 8.4 : V2-EVAL Terminal connection with 'Spy' connection enabled

4. Next open a connection to the 'Spy' channel on the V2-EVAL board. From the Vinculum logo pull down menu, select 'Connect to UART->VII Eval Board C' to open the UART connection to channel D on the FT4232H.

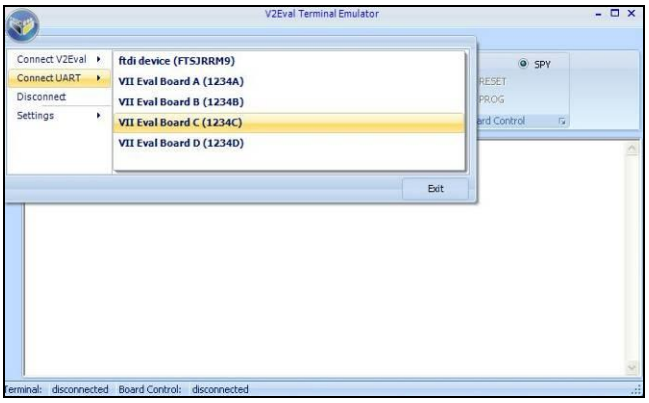


Figure 8.5 : Connect to 'Spy' channel on V2-EVAL board

The V2-EVAL board and software is now ready to display 'Spy' data being sent to the VNC2 device from an external device.

An example displaying 'Spy' mode operation is shown in Figure 8.6. The example displays 'Spy' mode operation with an FTDI USB to 3.3V TTL level UART cable connected to the V2-EVAL board via connector CN10. The terminal connection on the right represents the terminal connection for the FTDI TTL USB cable showing data being transmitted from this console to the V2-EVAL terminal utility in the background.

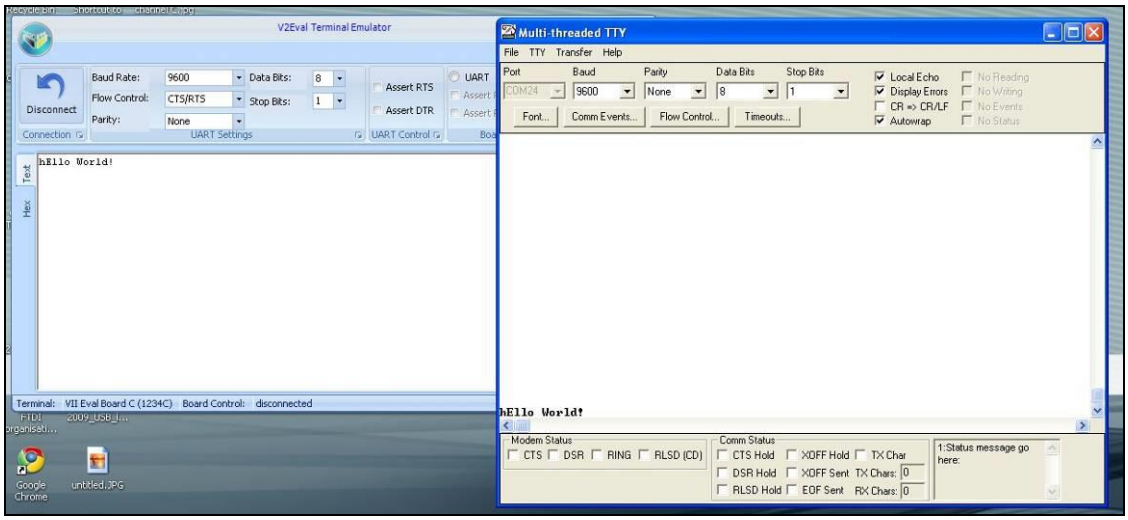
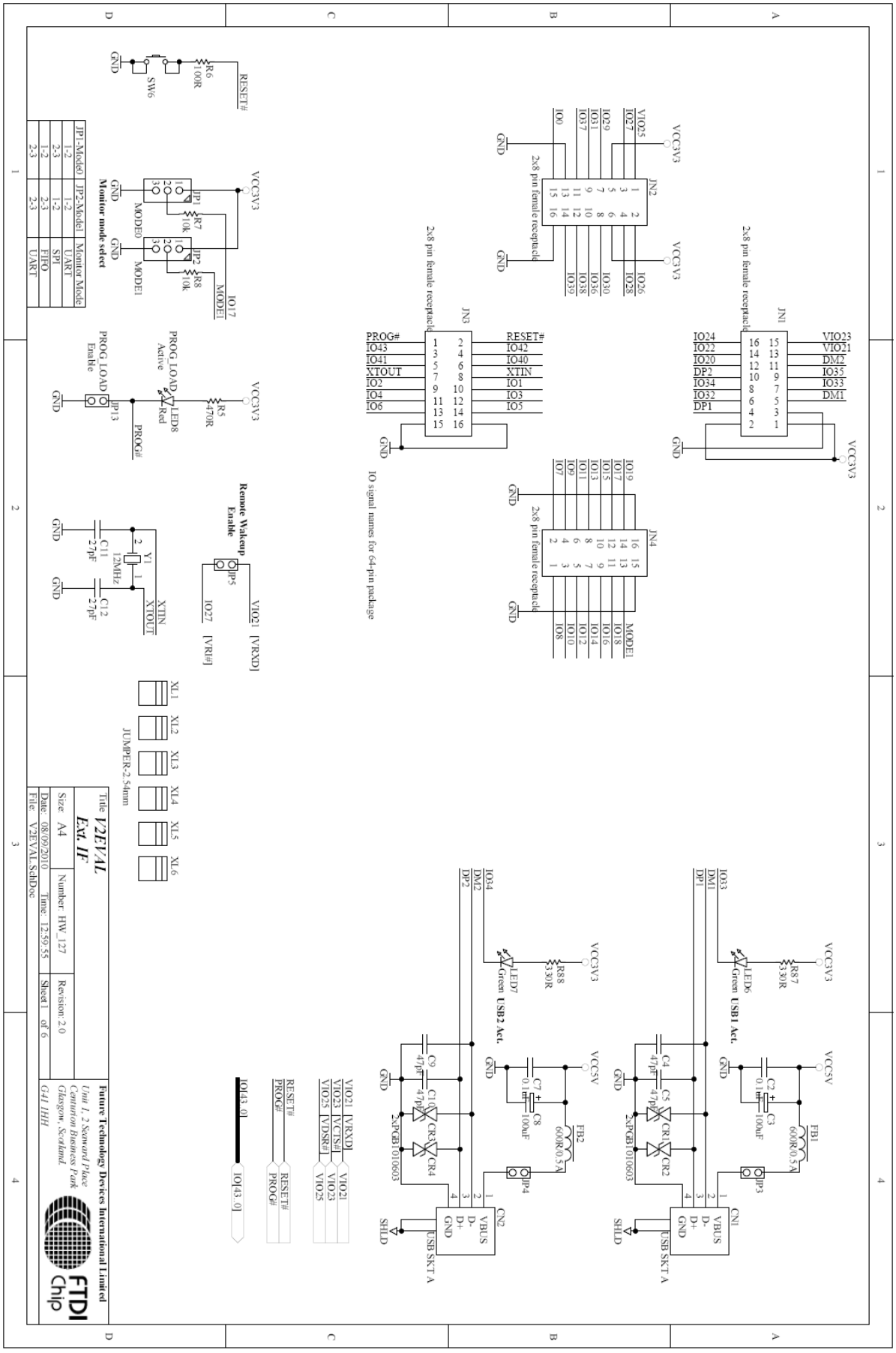


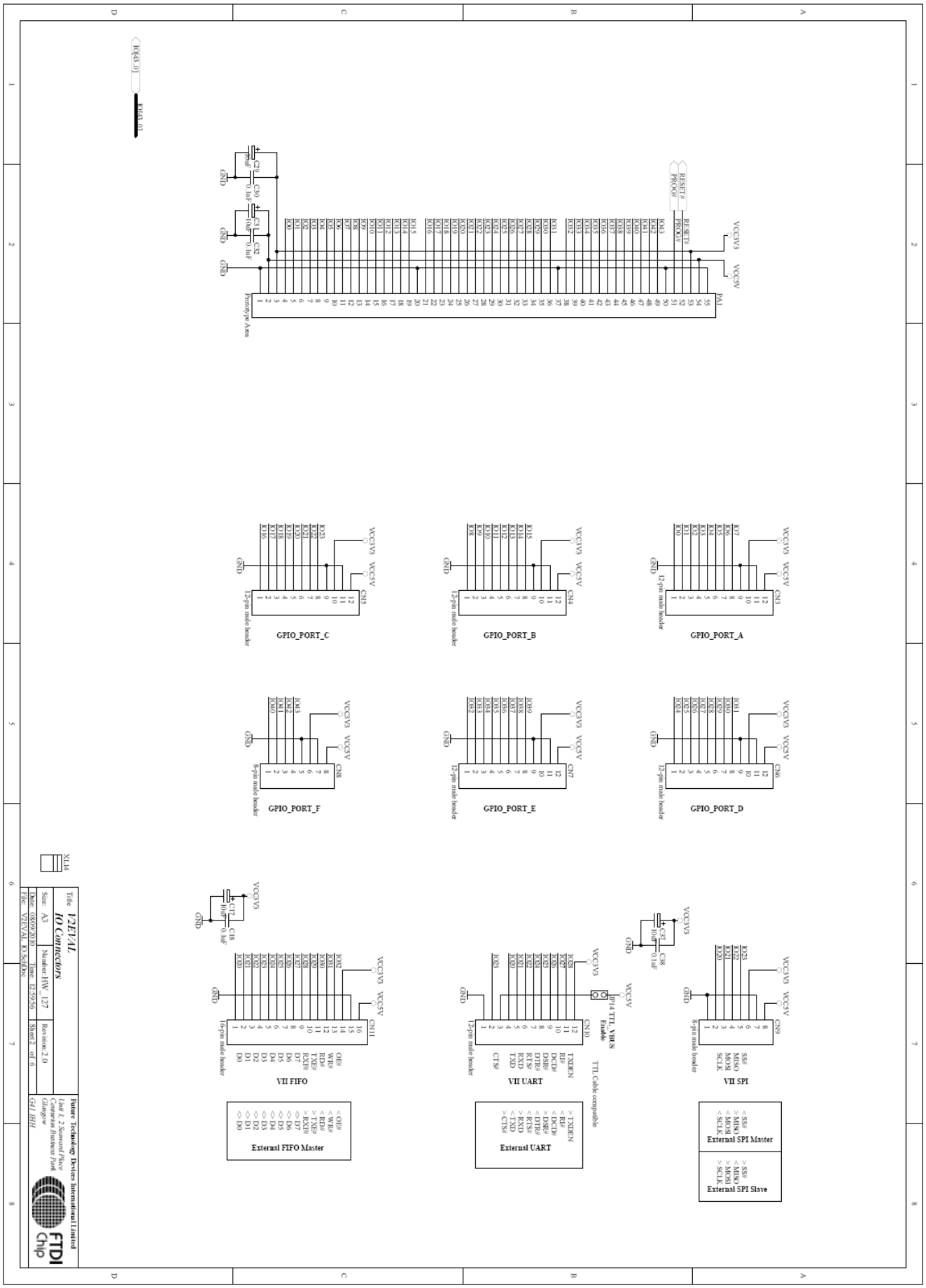
Figure 8.6 : 'Spy' mode operation

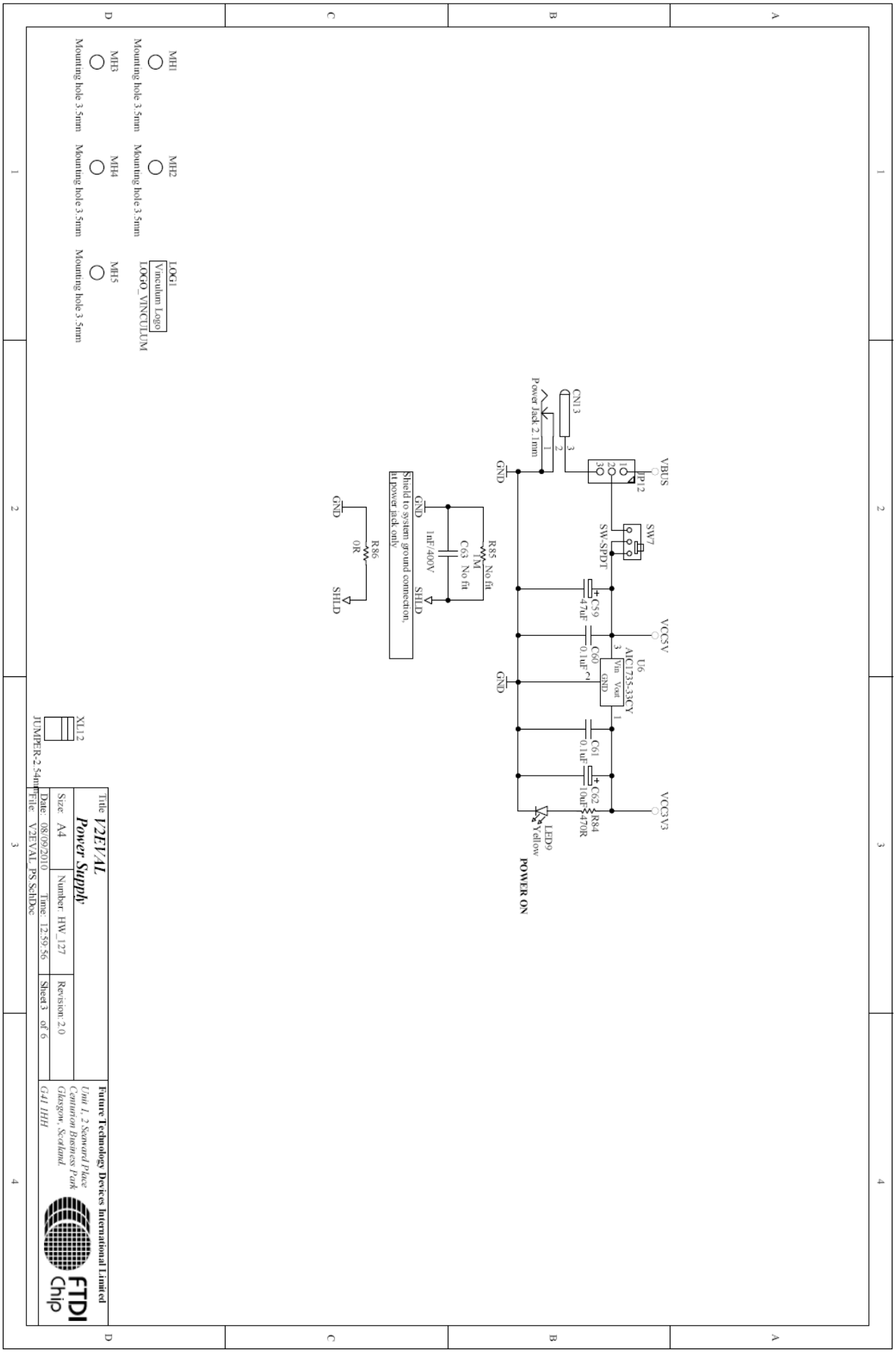
9 Board Schematics.

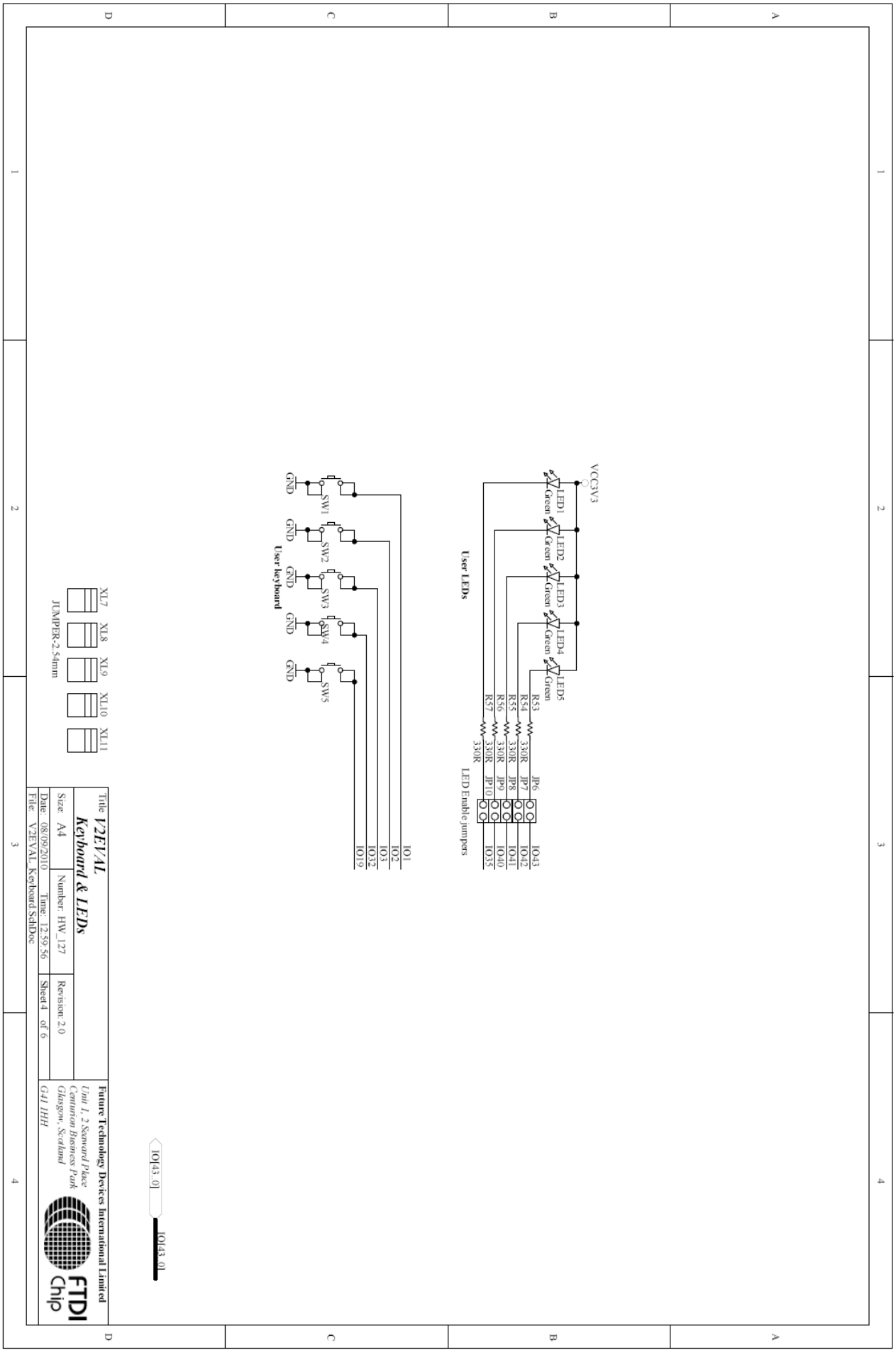
Schematics for the V2-EVAL board and VNC2 daughterboards are found in the following section.

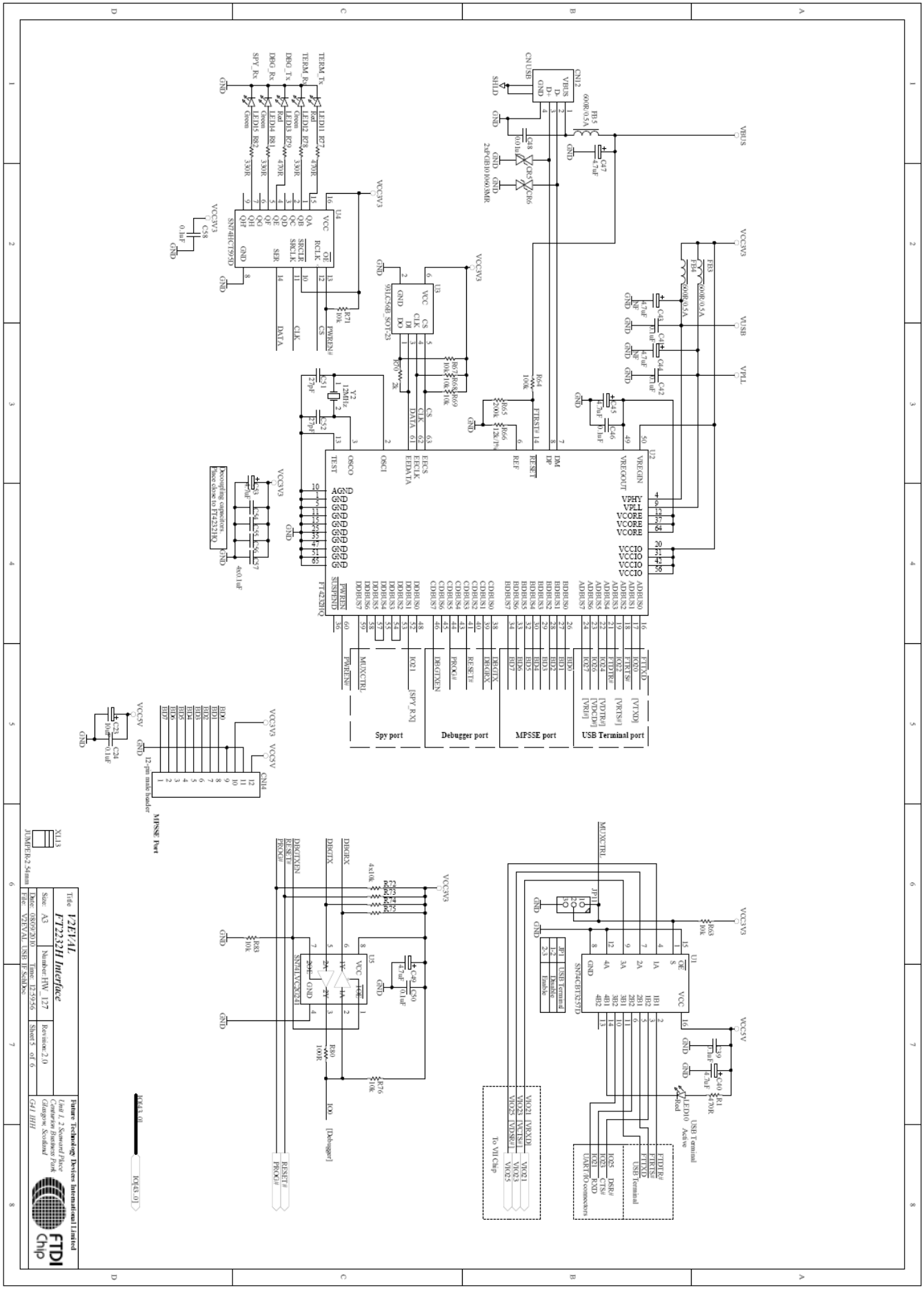
9.1 V2-EVAL Board Schematics



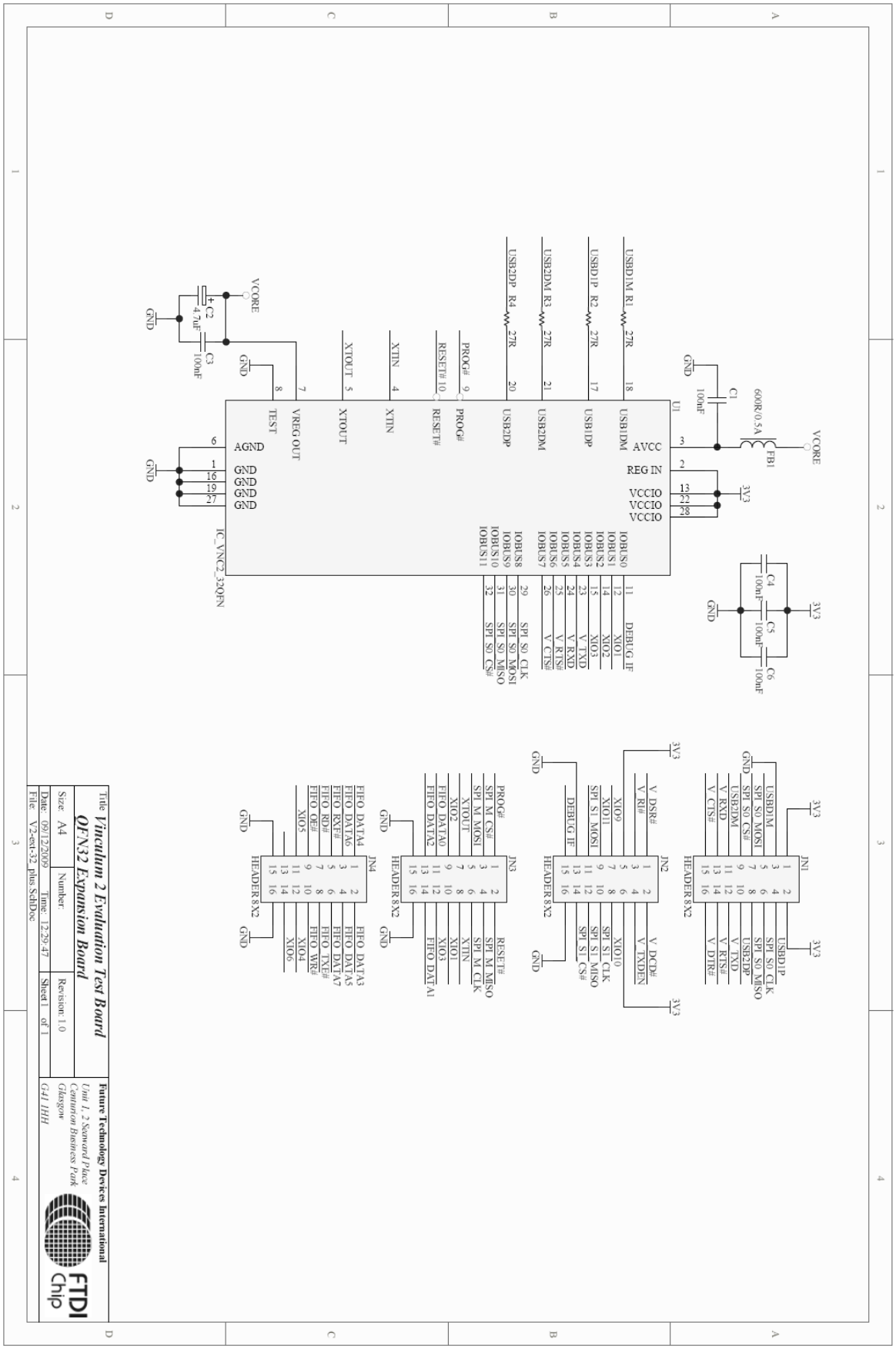

IO[63..0]
RESET#
PROG#
Prototype Area
GPIO_PORT_C
GPIO_PORT_B
GPIO_PORT_A
GPIO_PORT_F
GPIO_PORT_E
GPIO_PORT_D
VII FIFO
VII UART
VII SPI
External FIFO Master
External UART
External SPI Master
External SPI Slave
TTL Cable compatible
Future Technology Devices International Limited
V2EVAL
IO Connectors
Number HW: 127
Revision: 2.0
Sheet 2 of 6


MH1
Mounting hole 3.5mm
MH2
Mounting hole 3.5mm
MH3
Mounting hole 3.5mm
MH4
Mounting hole 3.5mm
MH5
Mounting hole 3.5mm
LOG1
Vinculum Logo
LOGO_VINCULUM
VBUS
JP12
SW7
SW-SPDT
CN13
Power Jack 2.1mm
GND
C59
47uF
C60
0.1uF
U6
AIC1735-33CY
Vin
Vout
GND
VCC5V
C61
0.1uF
C62
10uF
R84
470R
VCC3V3
LED9
Yellow
POWER ON
R85
1M
No fit
C63
No fit
1nF/400V
SHLD
Shield to system ground connection, at power jack only
R86
0R
XL12
JUMPER-2.54mm
Title V2EVAL
Power Supply
Size A4
Number HW_127
Revision 2.0
Date 08/09/2010
Time 12:59:56
Sheet 3 of 6
File V2EVAL_PS.SchDoc
Future Technology Devices International Limited
Unit 1, 2 Seaward Place
Centurion Business Park
Glasgow, Scotland
G41 1HH
FTDI Chip

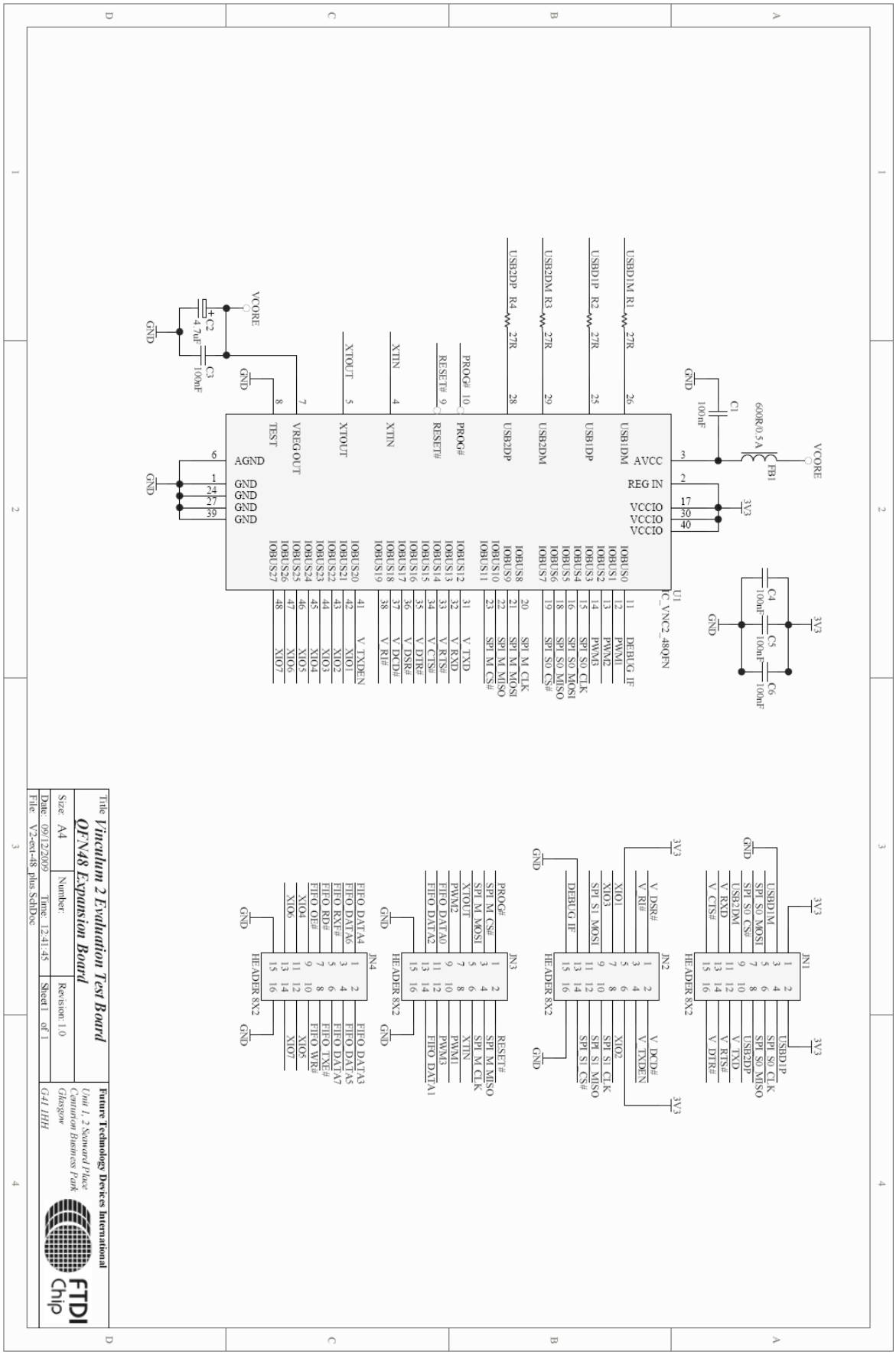

VCC3V3
LED1
LED2
LED3
LED4
LED5
Green
R53
R54
R55
R56
R57
330R
User LEDs
JP6
JP7
JP8
JP9
JP10
LED Enable jumpers
IO43
IO42
IO41
IO40
IO35
SW1
SW2
SW3
SW4
SW5
GND
User keyboard
IO1
IO2
IO3
IO32
IO19
XL7
XL8
XL9
XL10
XL11
JUMPER-2.54mm
IO[43..9]
IO[43..0]
Title V2EVAL
Keyboard & LEDs
Size: A4
Number: HW_127
Revision: 2.0
Date: 08/09/2010
Time: 12:59:56
Sheet 4 of 6
File: V2EVAL_Keyboard.SchDoc
Future Technology Devices International Limited
Unit 1, 2 Seaward Place
Centurion Business Park
Glasgow, Scotland
G41 1HH
FTDI Chip


Spy port
Debugger port
MPSSE port
USB Terminal port
MPSSE Port
Future Technology Devices International Limited
Unit 1, 2 Seaward Place
Centurion Business Park
Glasgow, Scotland
G41 1HH
Title: V2EVAL
FT2232H Interface
Size: A3
Number: EW_127
Revision: 2.0
Date: 08/09/2010
Time: 12:59:56
Sheet 5 of 6
File: V2EVAL_1SB_JP_SolDoc

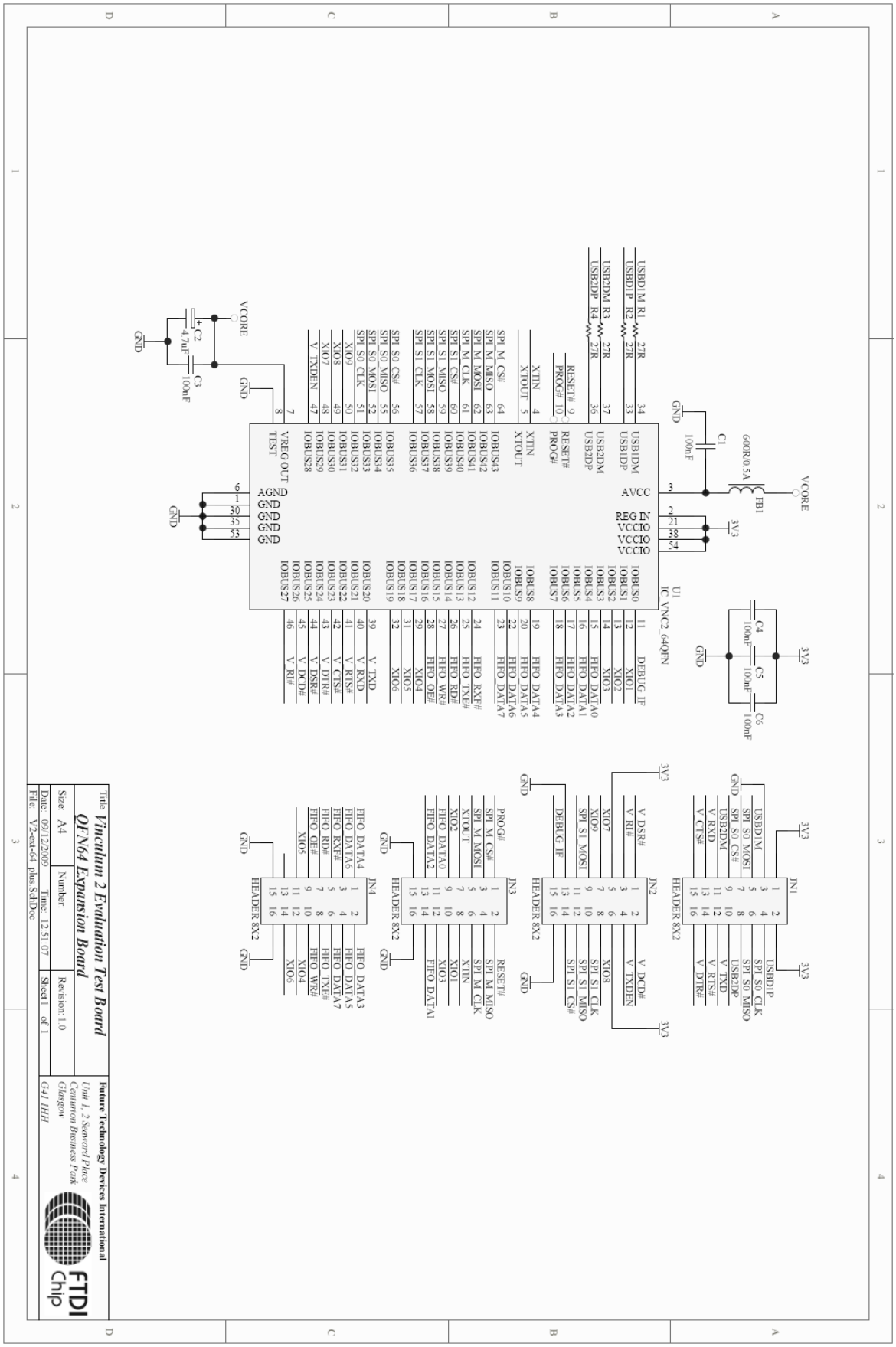
9.2 VNC2 Daughterboard - 32-pin QFN Schematic



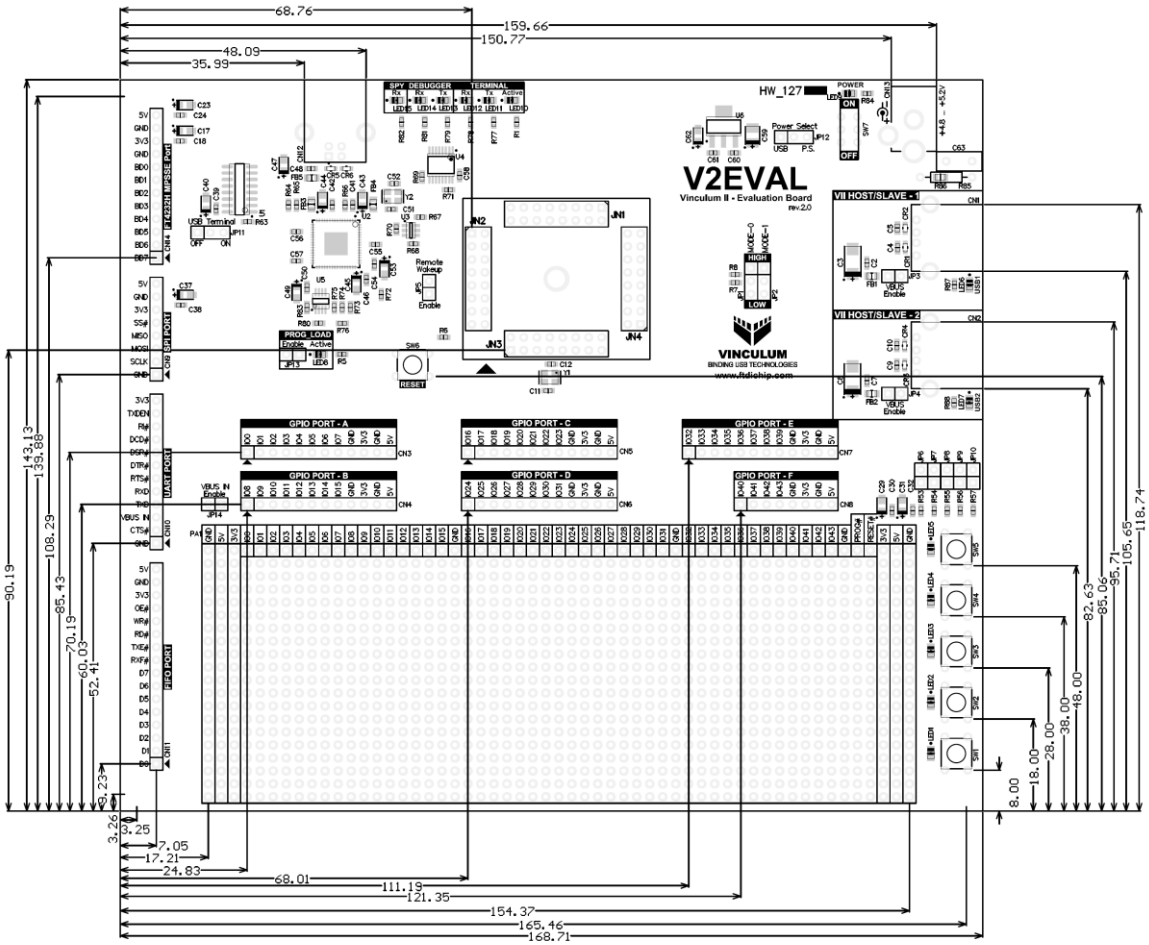
9.3 VNC2 Daughterboard - 48-pin QFN Schematic



9.4 VNC2 Daughterboard - 64-pin QFN Schematic



10 V2-EVAL Board Assembly Drawing



Top Assembly Drawing

Dimensions in mm.Tolerance is ±0.1mm

Contact Information

Head Office – Glasgow, UK

Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com

Branch Office – Taipei, Taiwan

2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan, R.O.C.
Tel: +886 (0) 2 8797 1330
Fax: +886 (0) 2 8751 9737

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com

Branch Office – Tigard, Oregon, USA

7130 SW Fir Loop
Tigard, OR 97223
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com

Branch Office – Shanghai, China

Room 1103, No. 666 West Huaihai Road,
Changning District
Shanghai, 200052
China
Tel: +86 21 62351596
Fax: +86 21 62351595

E-mail (Sales) cn.sales@ftdichip.com
E-mail (Support) cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com

Web Site

http://www.ftdichip.com

Appendix A – List of Figures and Tables

List of Figures

List of Tables

Appendix B – Revision History

Rev 1.0	First Release	19th January 2011
Rev 1.01	Updated CN10 table, schematic and assembly drawing, these changes only affect CN10	31th January 2011
Rev 1.1	Edited Table 5.9 - WR# listed as pin 50 on the 64-pin package	09th January 2013
Rev 1.11	Corrected USB pin-out in tables 5.11 and 5.12	11th December 2014
Rev 2.0	Minor Template edits	23rd March 2015