LTC2378-20
2ppm Linearity, DC Accurate Driver

DESCRIPTION

Demonstration circuit 2135A shows a simple DC accurate ADC driver circuit that converts a ±10V single-ended input signal into a fully differential signal capable of driving the LTC2378-20 with a combined linearity error of only 2ppm. The LTC2378-20 is a low power, low noise 20-bit SAR ADC with a serial output that operates from a single 2.5V supply. The following text refers to the LTC2378-20 but applies to all parts in the family, the only difference being the maximum sample rate. The LTC2378-20 supports a ±5V fully differential input range with a 104dB SNR, consumes only 21mW and achieves ±2ppm INL max with no missing codes at 20 bits. The DC2135A is the PCB that goes with DN1032. Refer to this design note for the theory of operation for this demo circuit. An option for a pseudo-differential input drive is provided. The DC2135A can be used with either the DC890 or DC590 USB controllers. Use the DC890 if precise sampling rates are required or to demonstrate AC performance such as SNR, THD, SINAD and SFDR. Use the DC590 to look at DC performance or to generate histograms showing peak-to-peak noise. The demonstration circuit 2135A also is intended to show recommended grounding, component placement and selection, routing and bypassing for this ADC.

Design files for this circuit board are available at http://www.linear.com/demo/DC2135A

An LTspice Simulation of the ADC Driver is available at http://www.linear.com/LTC2378-20

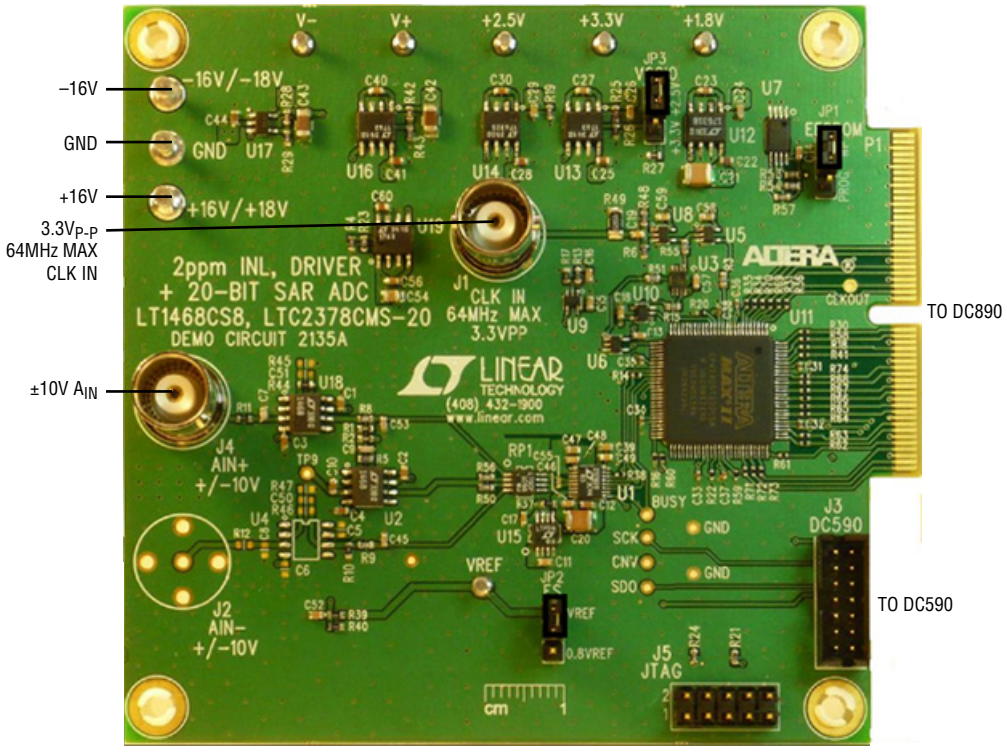


Figure 1. DC2135A Connection Diagram

DC890 QUICK START PROCEDURE

Check to make sure that all switches and jumpers are set as shown in the connection diagram of Figure 1. In particular make sure that VCCIO (JP3) is set to the 2.5V position. Operating the DC2135A with the DC890 while JP3 is in the 3.3V position will cause noticeable performance degradation in SNR and THD. The default connections configure the ADC to use the onboard reference and regulators to generate the required common mode voltages. The analog input is DC-coupled. Connect the DC2135A to a DC890 USB High Speed Data Collection Board using connector P1. Then, connect the DC890 to a host PC with a standard USB A/B cable. Apply ±16V to the indicated terminals. Then apply a low jitter sine source to J4. For the maximum recommended sampling rate of 800ksps connect a low jitter 64MHz 2.5V_{P-P} sine wave or square wave to connector J1. Note that J1 has a 50Ω termination resistor to ground.

Run the PScope™ software (PScope.exe version K75 or later) which can be downloaded from www.linear.com/software.

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The PScope software should recognize the DC2135A and configure itself automatically.

Click the Collect button (See Figure 4) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

DC590 QUICK START PROCEDURE

IMPORTANT! To avoid damage to the DC2135A, make sure that VCCIO (JP6) of the DC590 is set to 3.3V before connecting the DC590 to the DC2135A.

VCCIO (JP3) of the DC2135A should be in the 3.3V position for DC590 operation. To use the DC590 with the DC2135A, it is necessary to apply ±16V and ground to the appropriate terminals. Connect the DC590 to a host PC with a standard USB A/B cable. Connect the DC2135A to a DC590 USB serial controller using the supplied 14-conductor ribbon cable. Apply the signal source to J4.

Run the QuikEval™ software (version K101 or later) which can be downloaded from www.linear.com/software. The correct control panel will be loaded automatically. Click the COLLECT button (See Figure 5) to begin reading the ADC.

ASSEMBLY OPTIONS

Table 1. DC2135A Assembly Options

Assembly Version	U1 Part Number	Max Conversion Rate	Number of Bits	Max CLK IN frequency
DC2135A	LTC2378CMS-20	800ksps	20	64MHz

DC2135A SETUP

DC Power

The DC2135A requires ±16VDC and draws approximately 55mA. Most of the supply current is consumed by the CPLD, opamps, regulators and discrete logic on the board. The +16VDC input voltage powers the ADC through LT1763 regulators which provide protection against accidental reverse bias. Additional regulators provide power for the CPLD and opamps. See Figure 1 for connection details.

Clock Source

You must provide a low jitter $2.5V_{P-P}$ sine or square wave to J1. If VCCIO is in the 3.3V position, the clock amplitude should be $3.3V_{P-P}$. The clock input is AC-coupled so the DC level of the clock signal is not important. A clock generator like the Rohde & Schwarz SMB100A is recommended. Even a good clock generator can start to produce noticeable jitter at low frequencies. Therefore it is recommended for lower sample rates to divide down a higher frequency clock to the desired input frequency. The ratio of clock frequency to conversion rate is 80:1. If the clock input is to be driven with logic, it is recommended that the 50Ω terminator (R49) be removed. Slow rising edges may compromise the SNR of the converter in the presence of high-amplitude higher frequency input signals.

Data Output

Parallel data output from this board (0V to 2.5V default), if not connected to the DC890, can be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use pin 50 of P1 to latch the data. The data can be latched using either edge of this signal. The data output signal levels at P1 can also be changed to 0V to 3.3V if the application circuit requires a higher voltage. This is accomplished by moving VCCIO (JP3) to the 3.3V position.

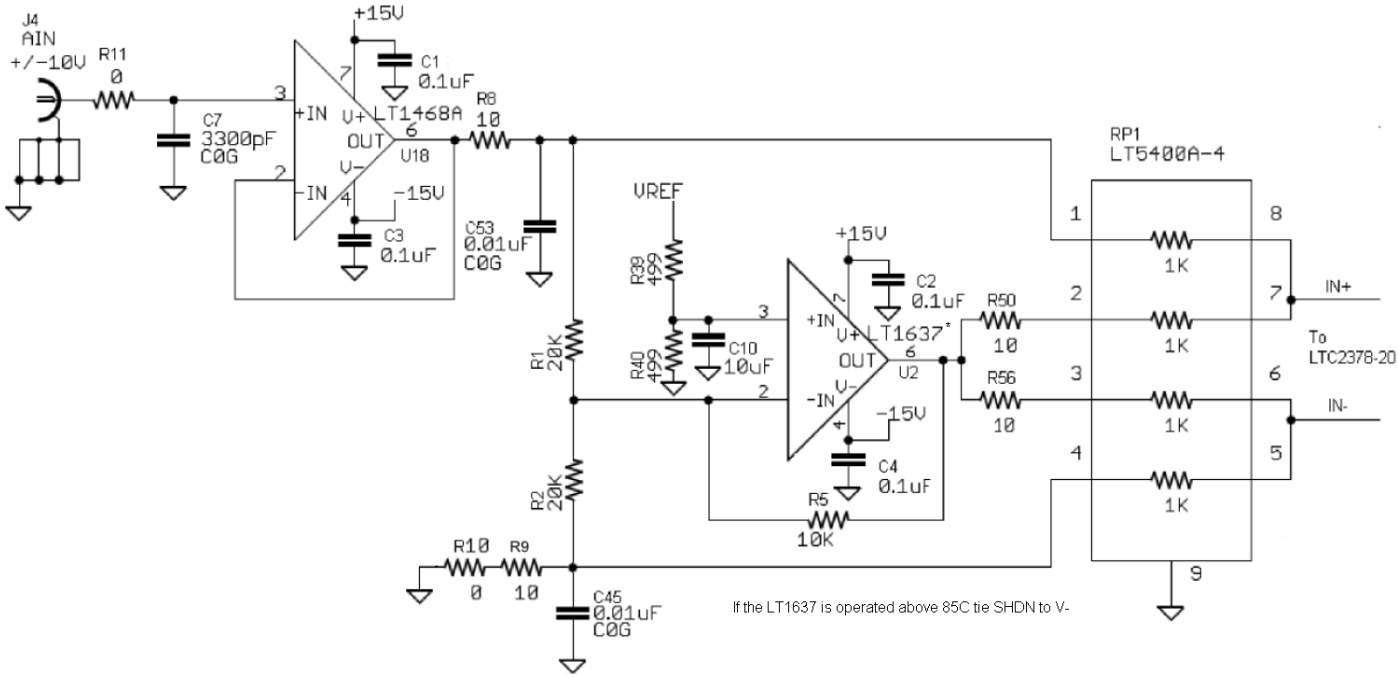


Figure 2. Default DC2135A Single-Ended Driver

DC2135A SETUP

Reference

The default reference is a LTC6655 5V reference. If an external reference is used it must settle quickly in the presence of glitches on the REF pin. To use an external reference, unsolder R37 and apply the reference voltage to the V_{REF} terminal.

Analog Input

The default input circuit for the DC2135A is shown in Figure 2. This circuit buffers a single-ended ±10V input signal applied at A_{IN}^+ and converts it to the differential signal required by the LTC2378-20 inputs. In addition, this circuit bandlimits the input frequencies to approximately 600kHz.

Alternatively, the circuit can be driven pseudo-differentially to reduce common mode noise as shown in the circuit of Figure 3. The circuit in Figure 3 can be implemented on the DC2135A by removing R10 and adding C5, C6, C8, J2, R12, R46 and U4. At this point it will be necessary to drive A_{IN}^+ (J4) and A_{IN}^-(J2).

Data Collection

For SINAD, THD or SNR testing a low noise, low distortion differential output sine generator such as the Stanford Research SR1 should be used. A low jitter RF oscillator such as the Rohde & Schwarz SMB100A is used as the clock source.

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with a frequency, that is a submultiple of the sample rate, and which will only exercise a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and N/2. Multiply M/N by the sample rate to obtain the input sine wave frequency. Another scenario that can yield poor results is if you do not have a sine generator capable of ppm frequency accuracy or if it cannot be locked to the clock frequency. You can use an FFT with windowing to reduce the "leakage" or spreading of the fundamental, to get a close approximation of the ADC performance. If windowing is required, the Blackman-Harris 92dB window is recommended. If an amplifier or clock source with poor phase noise is used, windowing will not improve the SNR.

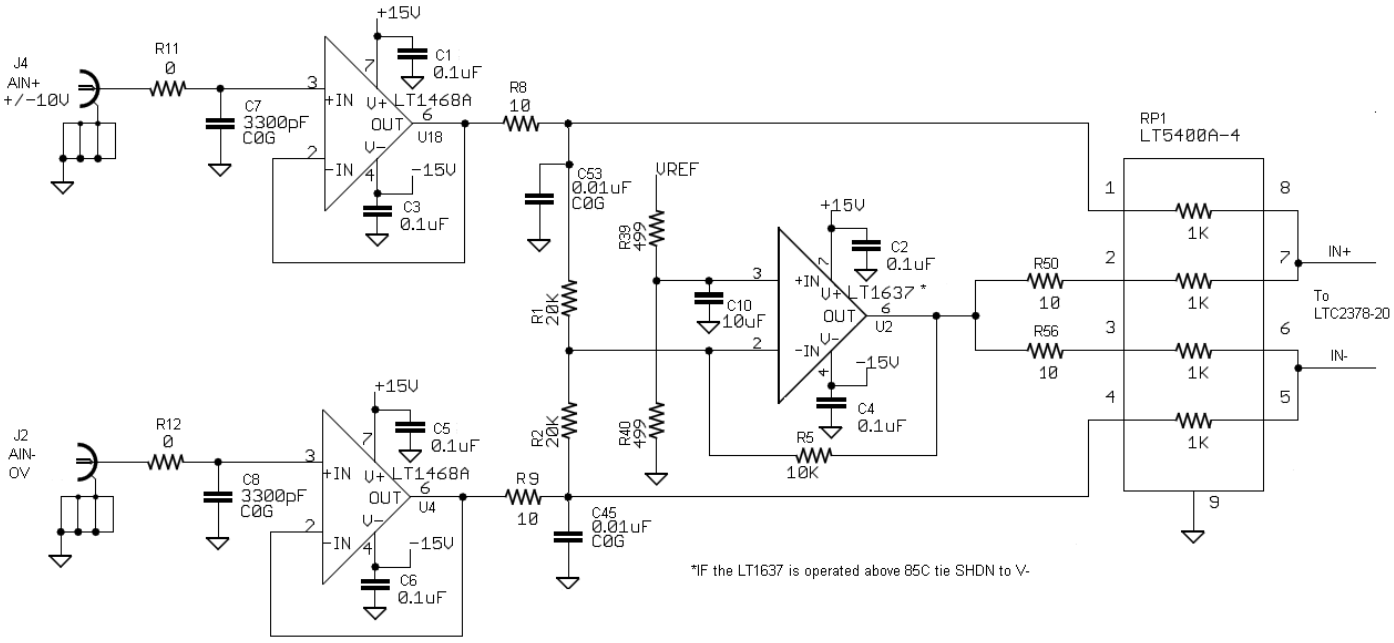


Figure 3. Pseudo-Differential Driver

DC2135A SETUP

To determine the performance of this demo board an inverse Fourier transform plot from PScope such as that shown in Figure 12 of this demo manual is used. This involves using a 64MHz clock source which yields a sample rate of 800ksps, along with a sinusoidal generator at an M/N(16/131072) frequency of 97.65625Hz. Windowing will not work in this application which requires vector averaging. The input signal level is approximately –1dBFS. After collecting a data sample like the one shown in Figure 4 remove the fundamental in the IFT mask by selecting the Edit IFT Mask button as shown in Figure 6. Zoom in on the mask so that the fundamental and harmonics are easily distinguishable as shown in Figure 7 and set the attenuation to 125dB. Click and drag the mouse across the fundamental to attenuate it. At this point the waveform should resemble Figure 8. Click the Done button. This will turn on the Display IFT Results in the Primitive Wave window. Next, select Processing Options as shown in Figure 9 and set the number of FFTs Average to 100 and change the X-axis selection from Bin # to Frequency as shown in Figure 10. Click OK to exit this window. Turn on vector averaging by clicking the button shown in Figure 11. Click on the Collect button and wait for the 100 averages to accumulate. The inverse Fourier transform in the P-Wave window at this point should display the distortion components as shown in Figure 12. Taking the large number of samples allows the distortion components to be seen through the noise. Drawing an imaginary line through the middle of the remaining noise band the distortion is approximately ±1LSB (1LSB = 1.05ppm). Using this technique, linearity vs input frequency (Figure 13) and linearity vs sampling rate (Figure 14) were generated to show the useful operating range of this demo circuit. Input frequencies above 900Hz and sample rates above 800ksps start to degrade performance of this demo circuit.

Layout

As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on the DC2135A should be used as a guideline for placement, and routing of the various components associated with the ADC. Here are some things to remember when laying out a board for the LTC2378-20. A ground plane is necessary to obtain maximum performance. Keep bypass capacitors as close to supply pins as possible. Use low impedance returns directly to the ground plane for each bypass capacitor. Use of a symmetrical layout around the analog inputs will minimize the effects of parasitic elements. Shield analog input traces with ground to minimize coupling from other traces. Keep traces as short as possible.

Component Selection

When driving a low noise, low distortion ADC such as the LTC2378-20, component selection is important so as to not degrade performance. Resistors should have low values to minimize noise and distortion. Metal film resistors are recommended to reduce distortion caused by self heating. Because of their low voltage coefficients, to further reduce distortion NPO or silver mica capacitors should be used.

DC2135A JUMPERS

Definitions

JP1: EEPROM is for factory use only. Leave this in the default WP position.

JP2: FS selects whether the Digital Gain Compression is on or off. In the V_{REF} position, Digital Gain Compression is off and the analog input range at A_{IN}^+ and A_{IN}^- is 0V to V_{REF}. In the $0.8V_{REF}$ position, Digital Gain Compression is turned on and the analog input range at A_{IN}^+ and A_{IN}^- is $0.1V_{REF}$ to $0.9V_{REF}$. The default setting is off.

JP3: VCCIO sets the output levels at P1 to either 3.3V or 2.5V. Use 2.5V to interface to the DC890 which is the default setting. Use 3.3V to interface to the DC590.

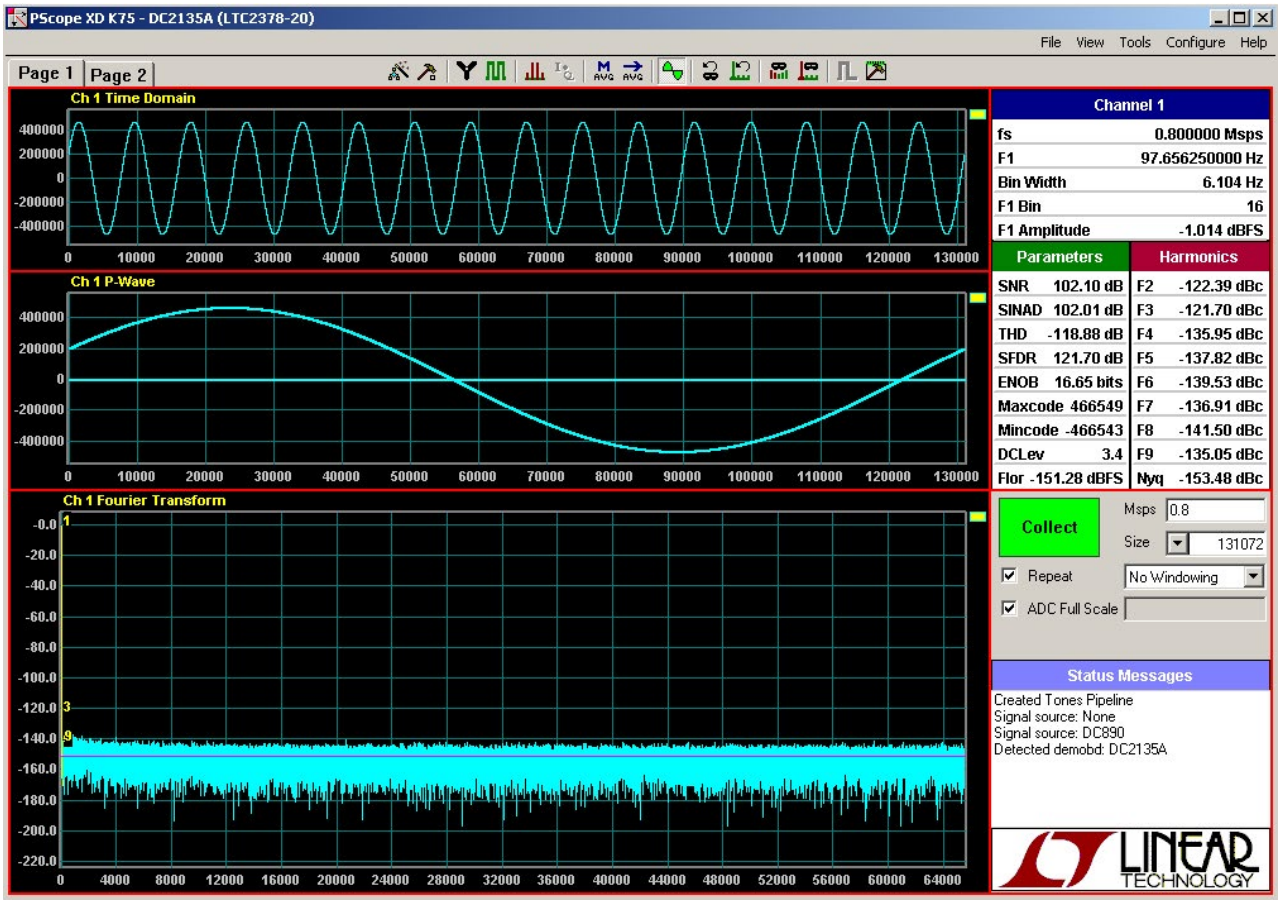


Figure 4. DC2135 PScope FFT

DC2135A JUMPERS

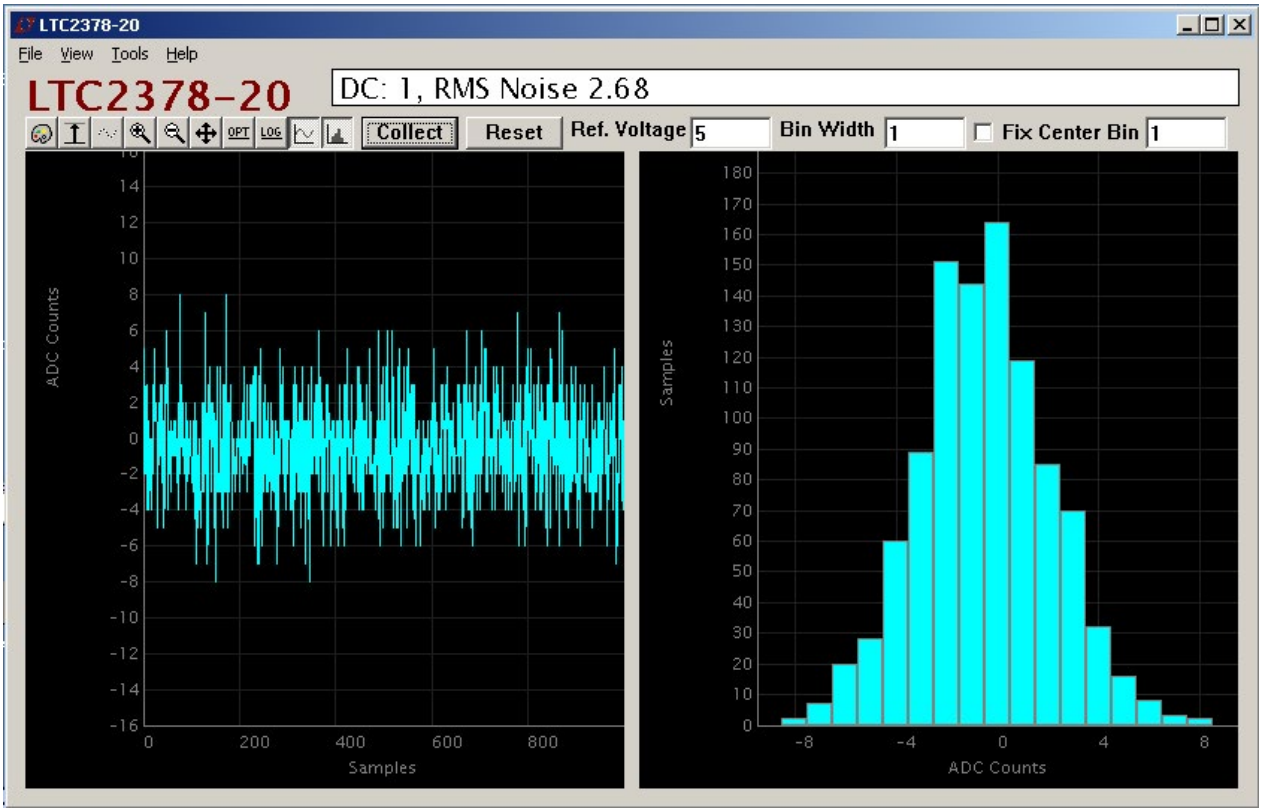


Figure 5. DC2135 QuikEval Histogram

DC2135A JUMPERS

Figure 6. Edit IFT Mask

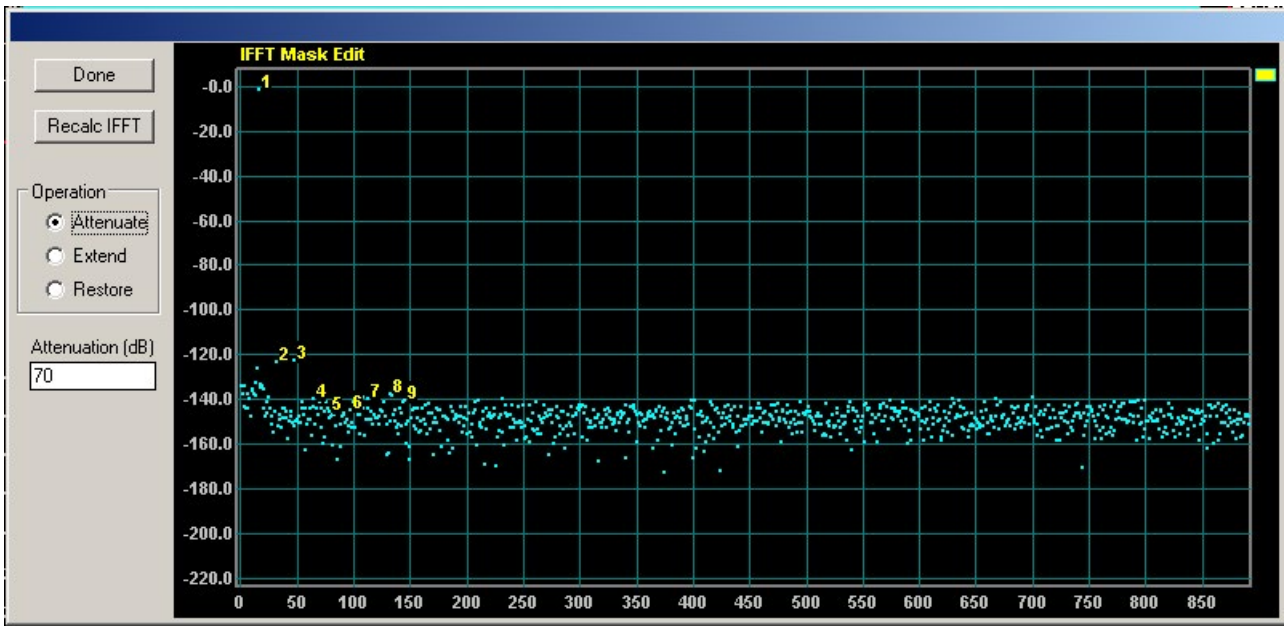


Figure 7. Unedited IFT Mask

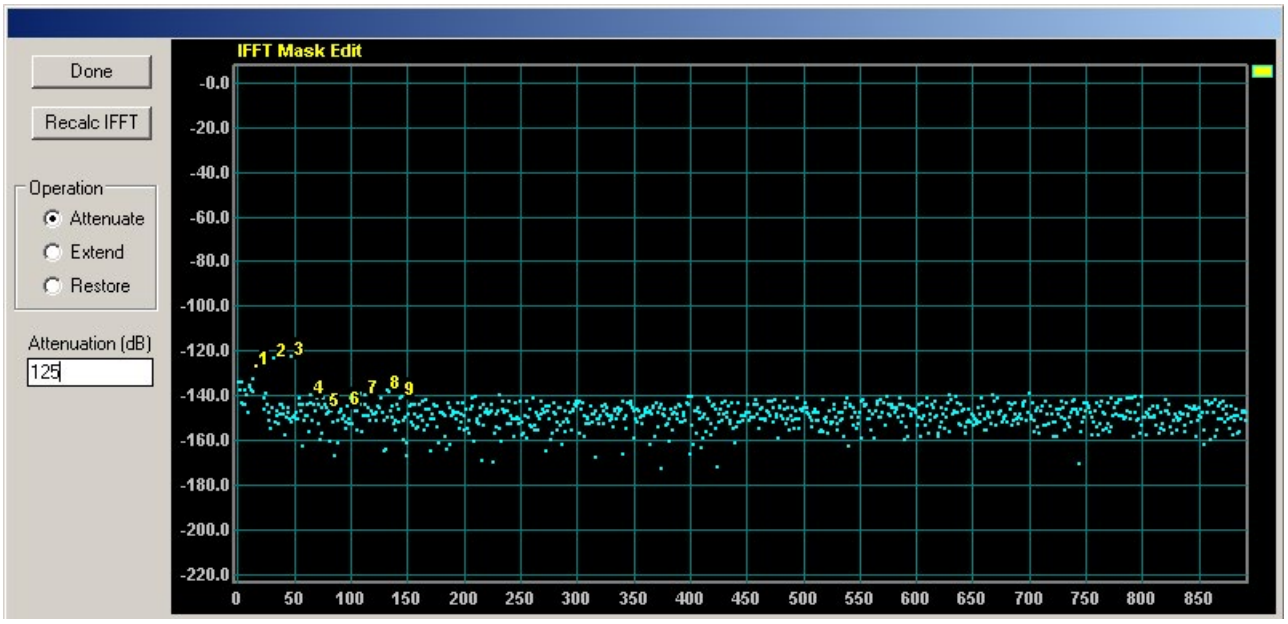


Figure 8. Edited IFT Mask with Fundamental Removed

DC2135A JUMPERS

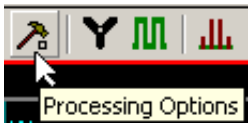


Figure 9. Processing Options Button

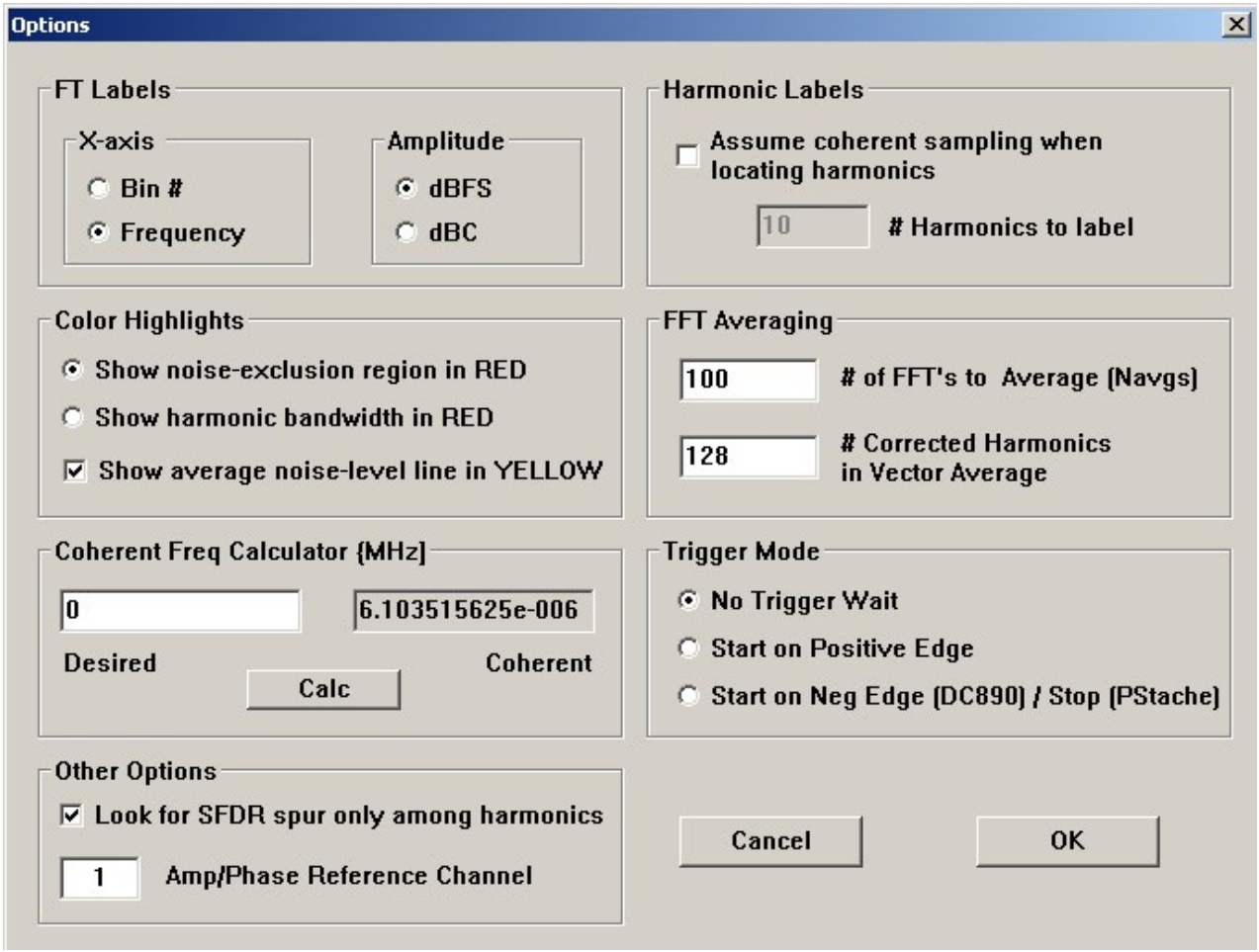


Figure 10. Processing Options with X-Axis Changed to Frequency and # of FFT's to Average Set to 100

DC2135A JUMPERS

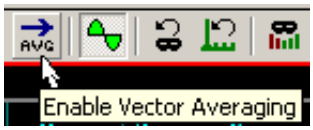


Figure 11. Enable Vector Averaging Button

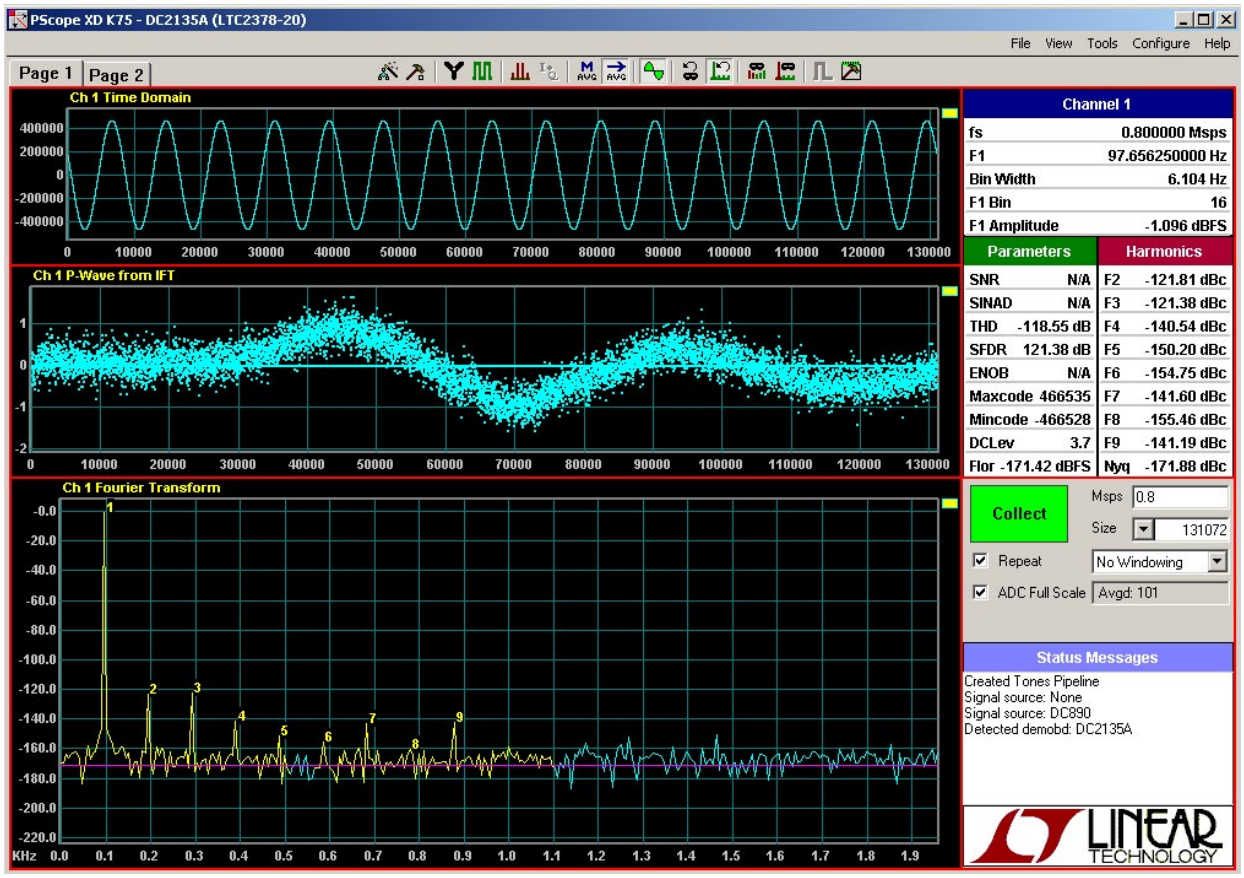


Figure 12. Distortion Components are Displayed in the PScope P-Wave Window

DC2135A JUMPERS

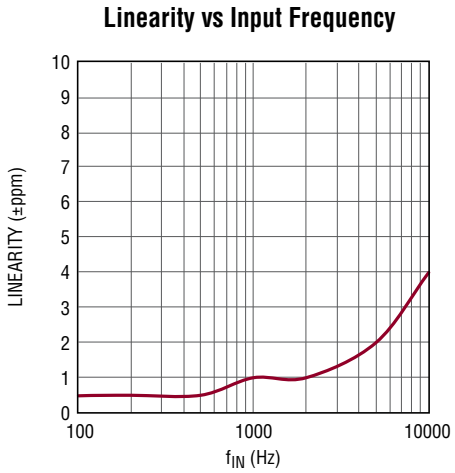


Figure 13. DC2135 Linearity vs Input Frequency

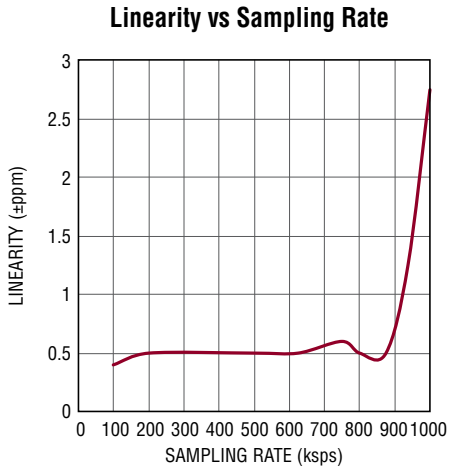


Figure 14. DC2135 Linearity vs Sampling Rate

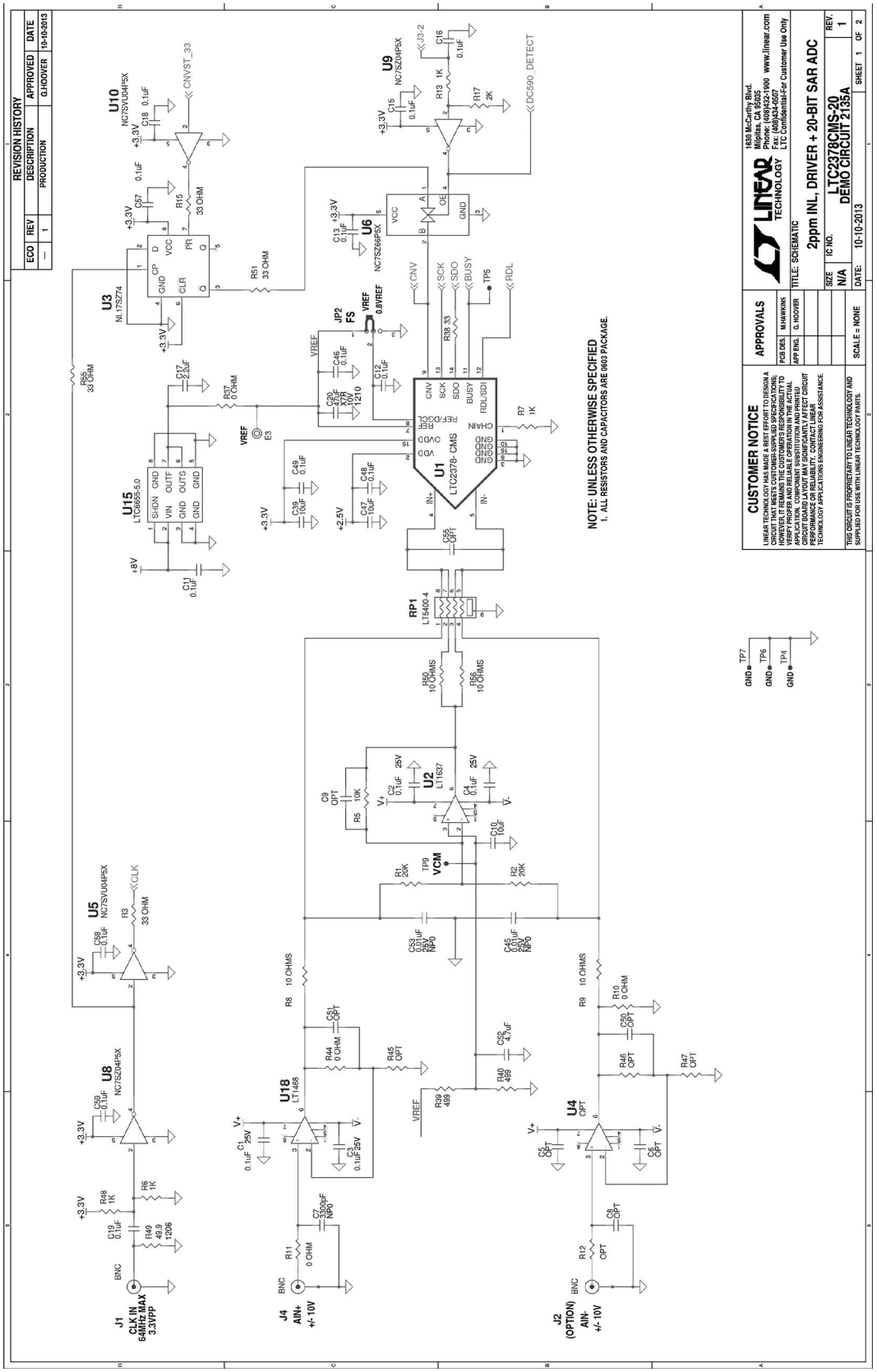
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	5	C1, C2, C3, C4, C12	CAP., X7R, 0.1µF, 25V, 20%, 0603	TDK, C1608X7R1E104M
2	0	C5, C6, C8, C9, C50, C51	CAP., OPT, 0603	OPTION
3	1	C7	CAP., NP0, 3300pF, 50V, 5%, 0603	MURATA GRM1885C1H332JA01D
4	1	C10	CAP., X5R, 10µF, 10V, 20%, 0603	SAMSUNG, CL10A106MP8NNNC
5	13	C11, C13, C14, C15, C16, C18, C19, C46, C48, C49, C57, C58, C59	CAP., X7R, 0.1µF, 16V, 10%, 0603	AVX, 0603YC104KAT2A
6	1	C17	CAP., X5R, 2.2µF, 10V, 10%, 0603	MURATA, GRM188R61A225KE34D
7	1	C20	CAP., X7R, 47µF, 10V, 10%, 1210	MURATA, GRM32ER71A476KE15L
8	1	C21	CAP., X5R, 22µF, 25V, 20%, 1210	MURATA, GRM32ER61E226ME15
9	6	C22, C25, C28, C41, C44, C60	CAP., X7R, 1µF, 25V, 10%, 0603	TDK, C1608X7R1E105K
10	5	C23, C27, C30, C40, C56	CAP., X7R, 0.01µF, 25V, 10%, 0603	MURATA, GRM188R71E103KA01D
11	5	C24, C26, C29, C39, C47	CAP., X5R, 10µF, 6.3V, 20%, 0603	AVX, 06036D106MAT2A
12	8	C31, C32, C33, C34, C35, C36, C37, C38	CAP., X7R, 0.1µF, 16V, 10%, 0402	TDK C1005X7R1C104K
13	2	C42, C43	CAP., X5R, 10µF, 25V, 10%, 1206	AVX, 12063D106KAT2A3L
14	2	C45, C53	CAP., NP0, 0.01µF, 25V, 5%, 0603	KEMET, C0603C103J3GACTU
15	1	C52	CAP., X5R, 4.7µF, 6.3V, 20%, 0603	TDK, C1608X5R0J475MT
16	1	C54	CAP., X5R, 10µF, 16V, 10%, 0805	MURATA, GRM21BR61C106KE15L
17	0	C55	CAP., OPT, 0402	OPTION
18	6	E1, E2, E3, E4, E5, E9	TEST POINT, TURRET, .061	MILL MAX, 2308-2-00-80-00-00-07-0
19	3	E6, E7, E8	TESTPOINT, TURRET, .094, PBF	MILL MAX, 2501-2-00-80-00-00-07-0
20	3	JP1, JP2, JP3	3 PIN SINGLE ROW HEADER, .100	SAMTEC, TSW-103-07-L-S
21	2	J1, J4	CONNECTOR, BNC	CONNEX, 112404
22	0	J2	CONNECTOR, BNC	CONNEX, 112404 (OPTION)
23	1	J3	HEADER, 2 × 7, 0.079"	MOLEX, 87831-1420
24	1	J5	HEADER, 2 × 5, 0.100"	SAMTEC, TSW-105-07-L-D
25	4	MH1, MH2, MH3, MH4	STANDOFF, NYLON 0.25"	KEYSTONE, 8831 (SNAP ON)
26	1	RP1	QUAD MATCHED RESISTOR NETWORK, MS8E	LINEAR TECH., LT5400ACMS8E-4#PBF
27	2	R1, R2	RES., CHIP, 20k, 1/10W, 1%, 0603	YAGEO, RC0603FR-0720KL
28	4	R3, R15, R51, R55	RES., CHIP, 33Ω, 1/10W, 5%, 0603	PANASONIC, ERJ-3GEYJ330V
29	9	R4, R6, R7, R13, R19, R24, R29, R43, R48	RES., CHIP, 1k, 1/10W, 1%, 0603	YAGEO, RC0603JR-071KL
30	2	R5, R21	RES., CHIP, 10k, 1/10W, 1%, 0603	VISHAY, CRCW060310K0FKEA
31	4	R8, R9, R50, R56	RES., CHIP, 10Ω, 1/10W, 1%, 0603	YAGEO, RC0603FR-0710RL
32	4	R10, R11, R37, R44	RES., CHIP, 0Ω, 1/10W, 0603	YAGEO, RC0603JR-070RL
33	0	R12, R45, R46, R47	RES., CHIP, OPT, 0603	OPTION
34	24	R14, R18, R30, R31, R34, R35, R36, R38, R41, R58, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74	RES., CHIP, 33Ω, 1/16W, 5%, 0402	YAGEO, RC0402JR-0733RL
35	1	R16	RES., CHIP, 300Ω, 1/16W, 5%, 0402	YAGEO, RC0402JR-07300RL
36	2	R17, R32	RES., CHIP, 2k, 1/10W, 5%, 0603	YAGEO, RC0603JR-072KL
37	3	R20, R22, R59	RES., CHIP, 1k, 1/16W, 5%, 0402	YAGEO, RC0402JR-071KL

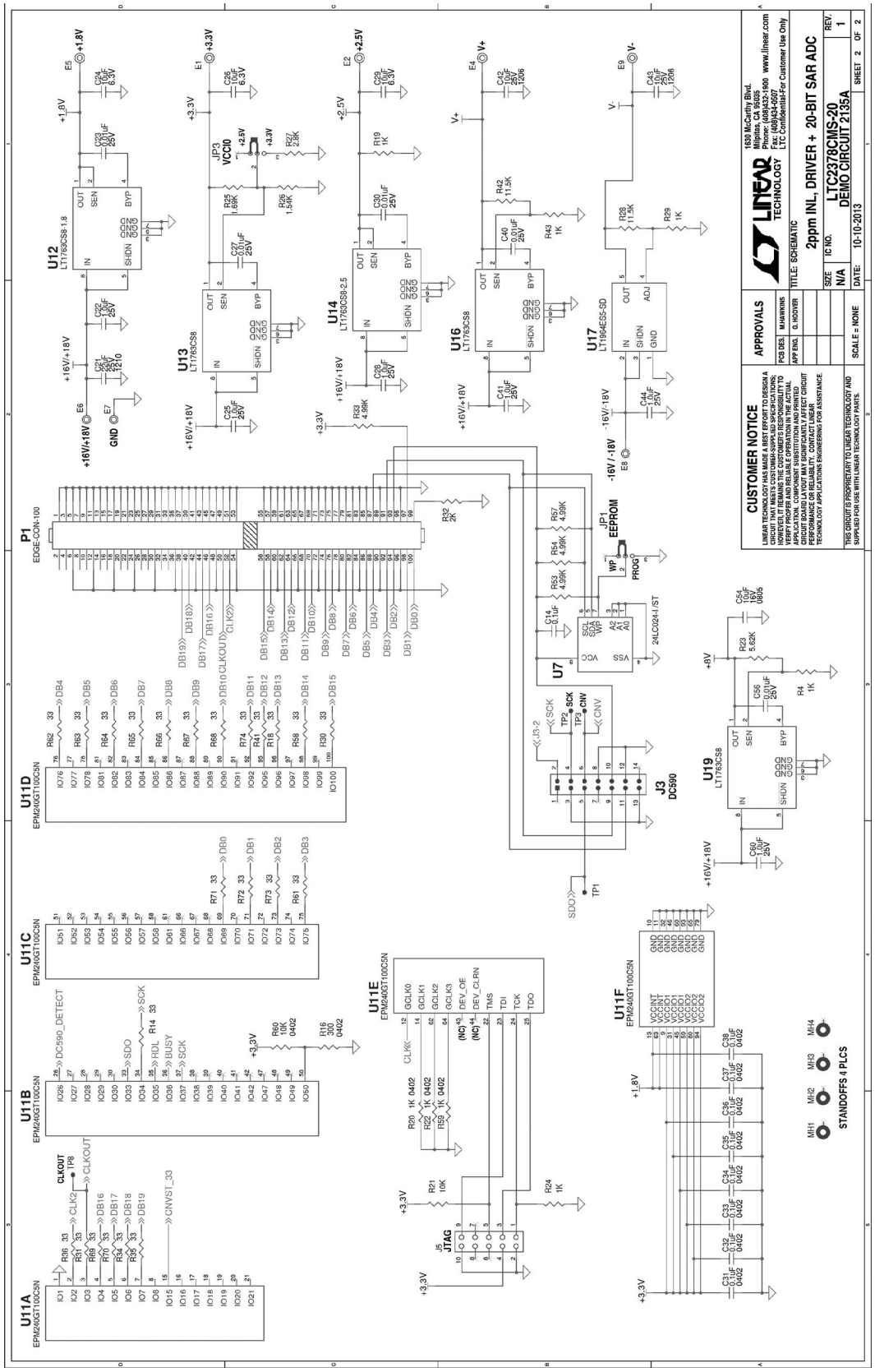
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
38	1	R23	RES., CHIP, 5.62k, 1/10W, 1%, 0603	YAGEO, RC0603FR-075K62L
39	1	R25	RES., CHIP, 1.69k, 1/10W, 1%, 0603	NIC, NRC06F1691TRF
40	1	R26	RES., CHIP, 1.54k, 1/10W, 1%, 0603	YAGEO, RC0603FR-071K54L
41	1	R27	RES., CHIP, 2.8k, 1/10W, 1%, 0603	YAGEO, RC0603FR-072K8L
42	2	R28, R42	RES., CHIP, 11.5k, 1/10W, 1%, 0603	YAGEO, RC0603FR-0711K5L
43	4	R33, R53, R54, R57	RES., CHIP, 4.99k, 1/10W, 1%, 0603	YAGEO, RC0603FRE074K99L
44	2	R39, R40	RES., CHIP, 499Ω, 1/10W, 1%, 0603	YAGEO, RC0603FR-07499RL
45	1	R49	RES., CHIP, 49.9Ω, 1/4W, 1%, 1206	VISHAY, CRCW120649R9FKEA
46	1	R60	RES., CHIP, 10k, 1/16W, 5%, 0402	YAGEO, RC0402JR-0710KL
47	1	U1	IC, HIGH SPEED, LOW NOISE SAR ADC	LINEAR TECH., LTC2378CMS-20#PBF
48	1	U2	IC, OP AMP, MICROPOWWR, SOIC	LINEAR TECH., LT1637CS8#PBF
49	1	U3	IC, D FLIP-FLOP, US8	ON SEMI., NL17SZ74USG
50	0	U4	IC, OP AMP, 90 MHZ, SOIC (OPTION)	LINEAR TECH., LT1468CS8#PBF
51	2	U5, U10	IC, UNBUFFERED INVERTER, SC70-5	FAIRCHILD, NC7SVU04P5X
52	1	U6	IC, SINGLE SPST BUS SWITCH, SC70-5	FAIRCHILD, NC7SZ66P5X
53	1	U7	IC, SERIAL EEPROM, TSSOP	MICROCHIP, 24LC024-I/ST
54	2	U8, U9	IC, UHS INVERTER, SC70-5	FAIRCHILD, NC7SZ04P5X
55	1	U11	IC, MAX II CPLD, TQFP100	ALTERA, EPM240GT100C5N
56	1	U12	IC, MICROPOWER REGULATOR, SO-8	LINEAR TECH., LT1763CS8-1.8#PBF
57	3	U13, U16, U19	IC, MICROPOWER REGULATOR, SO-8	LINEAR TECH., LT1763CS8#PBF
58	1	U14	IC, MICROPOWER REGULATOR, SO-8	LINEAR TECH., LT1763CS8-2.5#PBF
59	1	U15	IC, VOLTAGE REFERENCE, MSOP	LINEAR TECH., LTC6655BHMS8-5#PBF
60	1	U17	IC, MICROPOWER NEG. REGULATOR	LINEAR TECH., LT1964ES5-SD#PBF
61	1	U18	IC, OP AMP, 90MHz, SOIC	LINEAR TECH., LT1468CS8#PBF
62	3	XJP1, XJP2, XJP3	SHUNT, 0.100 CENTERS	SAMTEC, SNT-100-BK-G

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user releases LTC from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. Also be aware that the products herein may not be regulatory compliant or agency certified (FCC, UL, CE, etc.).

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LTC currently services a variety of customers for products around the world, and therefore this transaction **is not exclusive**.

Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035