CEL California Eastern Laboratories

Evaluation Board Document

µPG2159T6R-EVAL-A

Evaluation Board

- Description
- Insertion Loss of Through Board
- Performance Data Plots
- Assembly Drawing

Description:

The uPG2159T6R-EVAL-A evaluation board provides a quick and convenient means of evaluating the performance of the NEC uPG2159T6R switch. In addition to the device, the board provides DC block capacitors, power supply bypass capacitors, and RF and DC connectors.

A DC block capacitor is required at all RF ports. On this board, two parallel capacitors of 22pF are used for this purpose. This configuration minimizes the mismatch effect associated with the serial capacitors over a wide frequency range. In a real application where the operation frequency range is relatively narrow, one DC block capacitor usually is sufficient. The user should select the appropriate capacitor value according to the operation frequencies and the type of capacitor selected. Generally the performance of the switch circuit is not sensitive, to a certain extent, to the value of DC block capacitors.

A 1000pF capacitor is used for DC bypass on all control lines. For high speed applications the user may choose smaller capacitance or no capacitor at all.

DC supply connectors:

P1 is control voltage V_{cont1}, P2 is V_{cont2} and pins P3 and P4 are the ground.
V_{cont1} and V_{cont2} should be connected to separate power supplies to provide the required control logic.

RF connectors:

As indicated on the board, J1 is connected to the OUTPUT1 port, J2 is connected to the OUTPUT2 port and J3 is connected to the INPUT port.

Information on Board Material:

The board material is 20 mil thick Duroid 6002. Its dielectric constant is 2.94.

Switch Logic Table:

The following table lists the logic table for switch states.

Vcont1	Vcont2	INPUT – OUTPUT1	INPUT – OUTPUT2
H	L	ON	OFF
L	H	OFF	ON

Insertion Loss of Through Board:

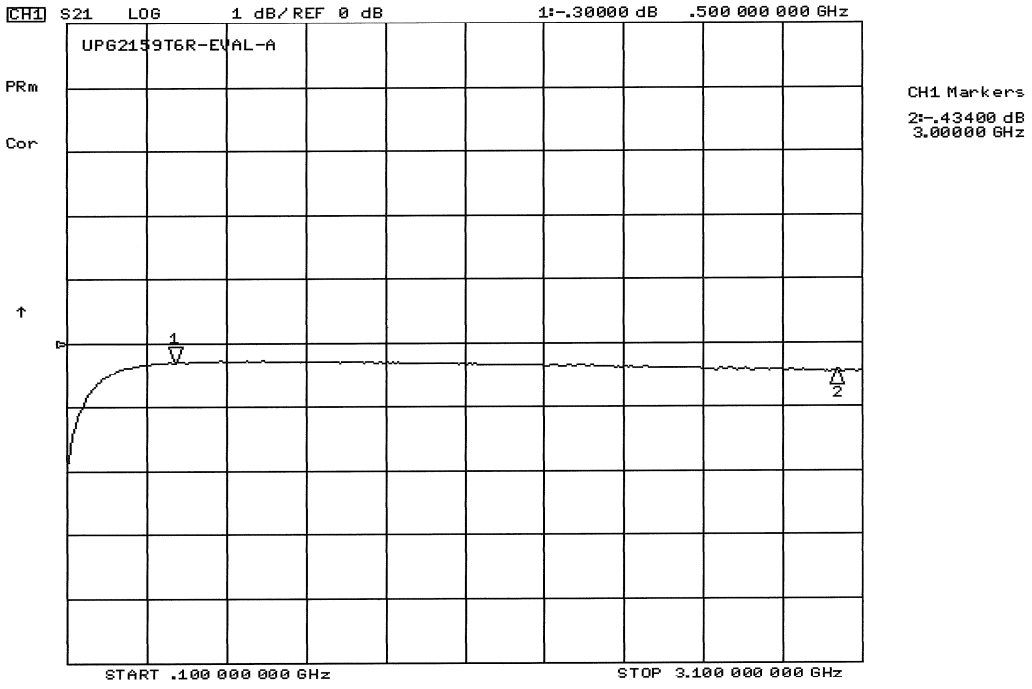
The insertion loss plot shown below is from direct measurement on an evaluation board. It is necessary to take the loss through the connectors and PCB trace into account in assessing the insertion loss through the switch alone. To this end a through board was characterized to determine the board/connector loss. The table below lists the board loss at different frequencies.

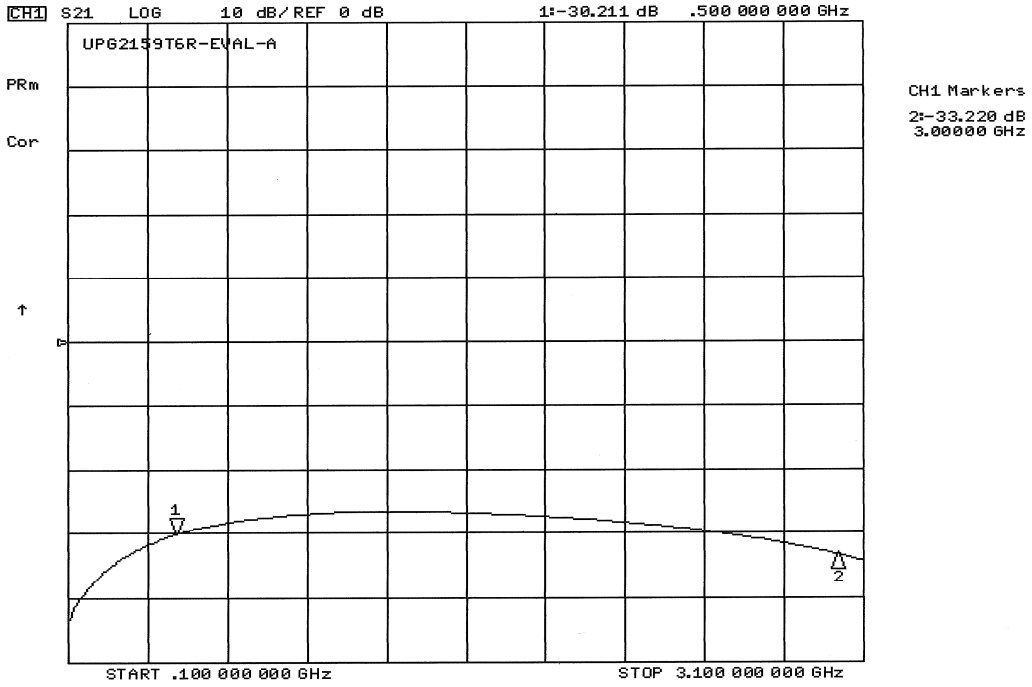
INPUT FREQUENCY (GHz)	BOARD LOSS (dB)
0.5	0.053
1.0	0.073
1.5	0.107
2.0	0.120
2.5	0.133
3.0	0.154

Performance Plots:

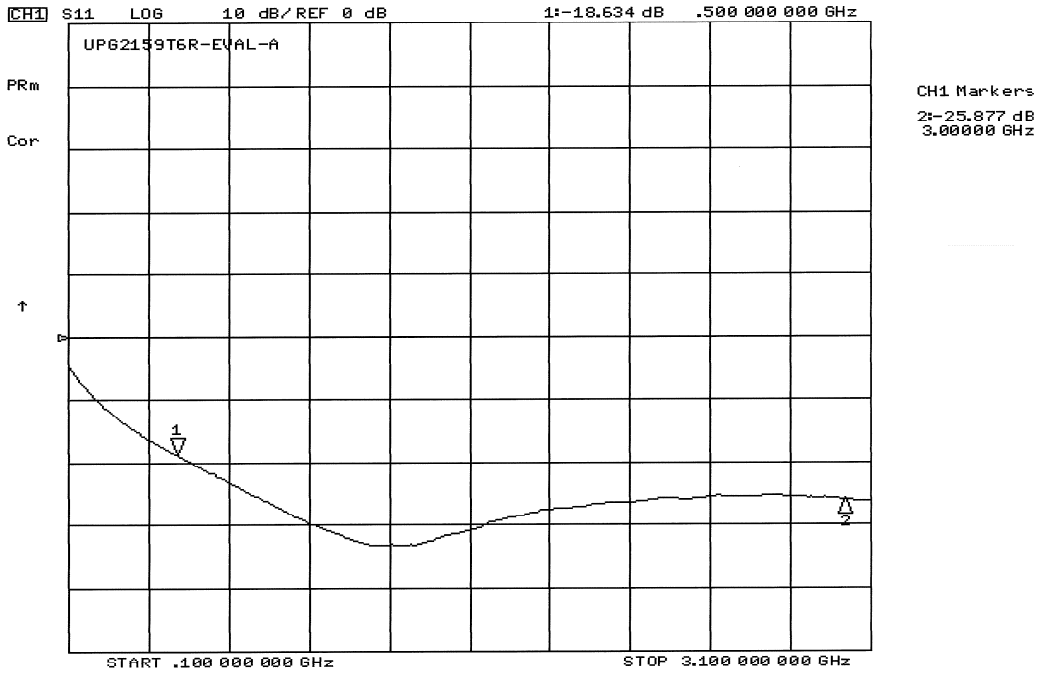
The following plots show typical data on insertion loss, isolation and return losses for the condition of INPUT to OUTPUT1 path being ON. The data for condition of INPUT to OUTPUT2 being ON is similar.

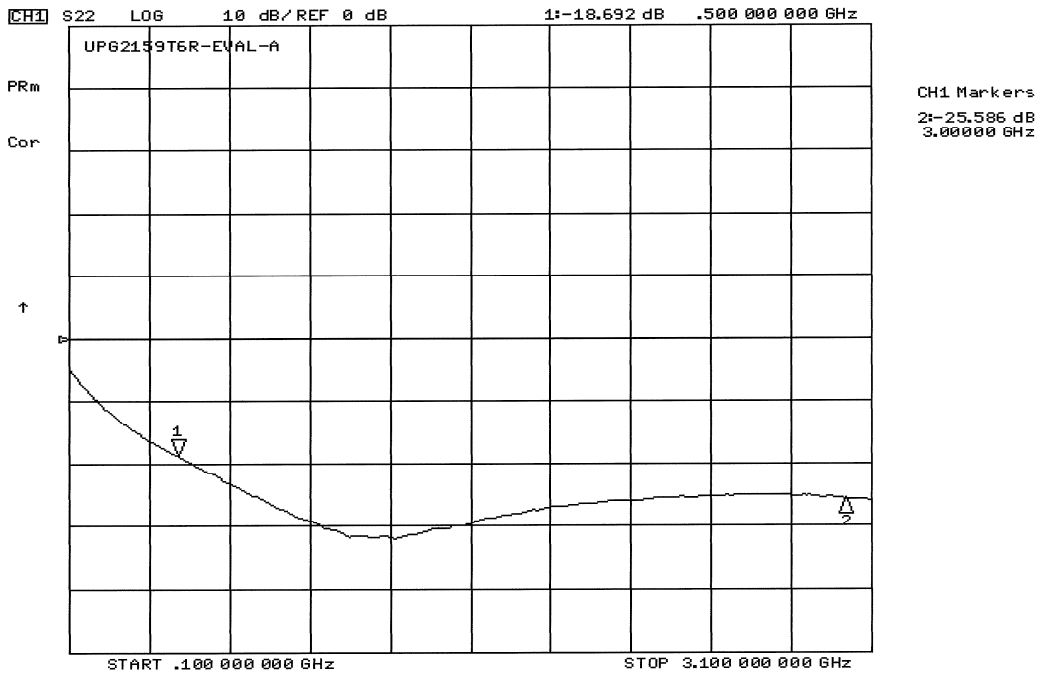
Insertion Loss and Isolation Plots



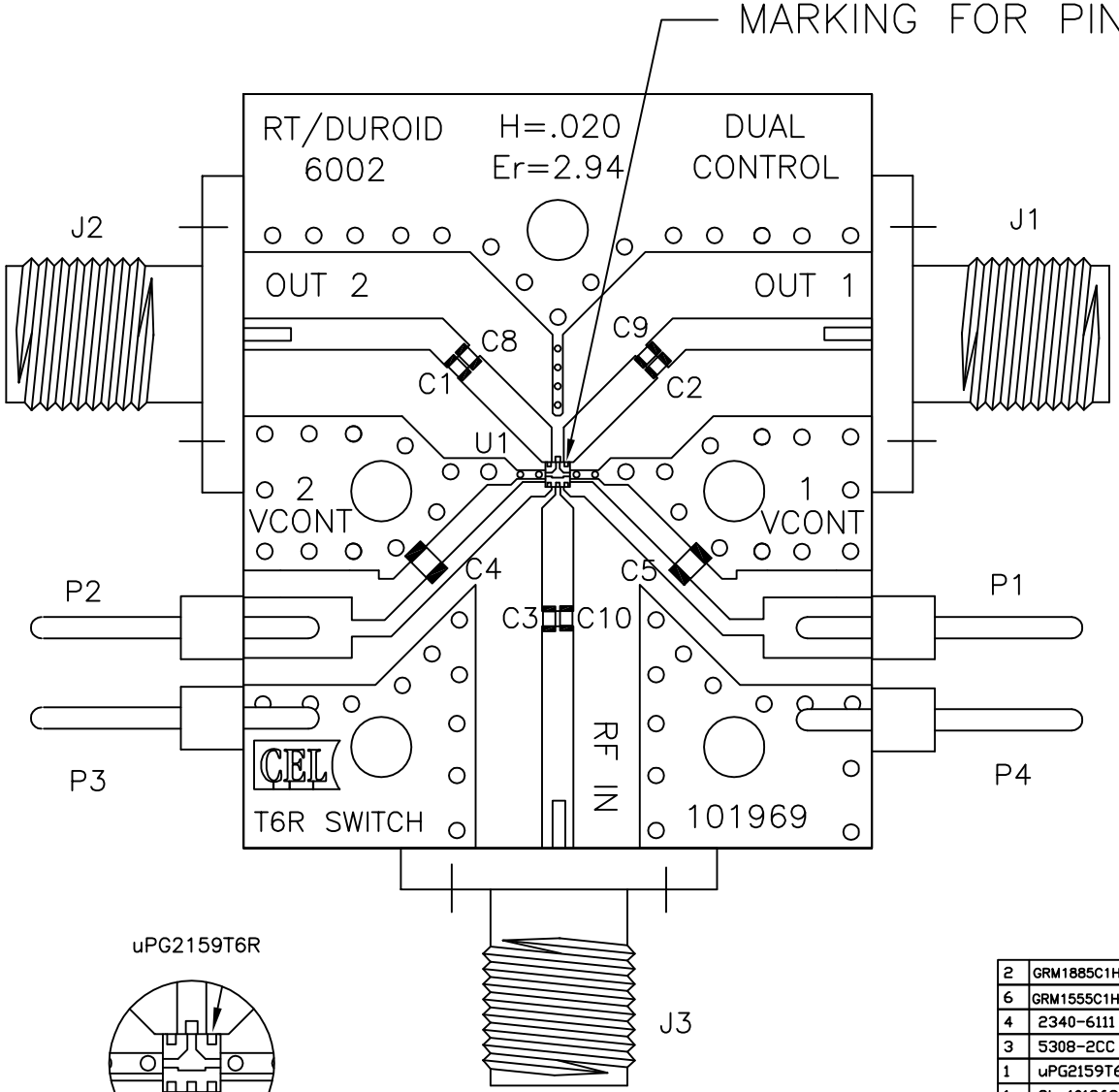


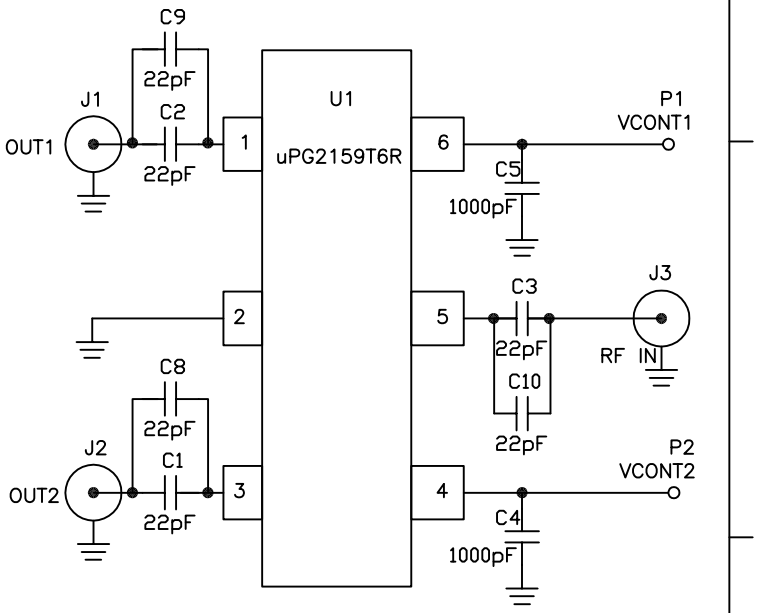
Input and Output Return Loss Plots





REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED





MARKING FOR PIN1
IS ON TOP OF CHIP

PACKAGE MARKING: G7

QTY	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
2	GRM1885C1H102JA01D	C4,C5	0603 1000pF CAP MURATA	6
6	GRM1555C1H220JZ01D	C1,C2,C3,C8,C9,C10	0402 22pF CAP MURATA	5
4	2340-6111 TG	P1,P2,P3,P4	PIN HEADER 3M	4
3	5308-2CC	J1,J2,J3	SMA FEMALE CONNECTOR TENSOLITE	3
1	uPG2159T6R	U1	IC NEC uPG2159T6R GaAs Switch	2
1	CL-101969	DRAWING	COMPONENT LAYOUT DRAWING	1

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX± .01 .XXX± .005
ANGULAR ± 1°
DO NOT SCALE DRAWING

MATERIAL

FINISH

APPROVALS		
Drawing by:	Bernard Urborg	02/06/2008
Designed by:	Bernard Urborg	02/06/2008
Checked by:		
Project Engineer:		
Quality Control:		

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TITLE:
ASSEMBLY DRAWING
uPG2159T6R-EVAL-A

SIZE	FSCM NO.	DWG NO.	REV
C		AD-101863	-

SCALE NONE	RELEASE DATE PROTOTYPE	SHEET 1 OF 1