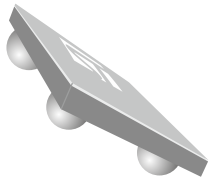
EMIF02-SPK01C2

2 line IPAD™, EMI filter including ESD protection

Datasheet - production data



Coated Flip-Chip package

Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency EMI filter (-33 dB @ 900 MHz)
- Very low PCB space consumption: 1.07 mm x 1.47 mm
- Very thin package: 0.670 mm
- Coating resin on back side and lead free package
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging.

Complies with the following standards:

- IEC 61000-4-2 level 4, on input pins:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC 61000-4-2 Level 1, on output pins:
  - 2 kV (air discharge)
  - 2 kV (contact discharge)
- MIL STD 883G - Method 3015-7 Class 3

Applications

Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Computers and printers and MCU Boards

Description

The EMIF02-SPK01C2 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The Flip-Chip packaging means the package size is equal to the die size. This filter includes ESD protection circuitry, which prevents damage to the application when it is subjected to ESD surges up to 15 kV.

Figure 1. Pin configuration (bump side)

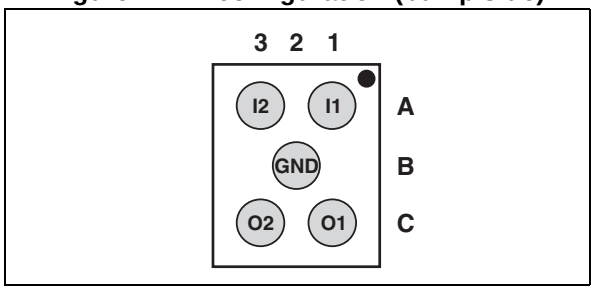
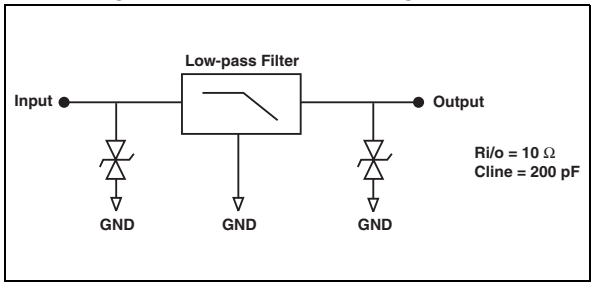


Figure 2. Basic cell configuration



TM: IPAD is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Figure 3. Electrical characteristics (definitions)

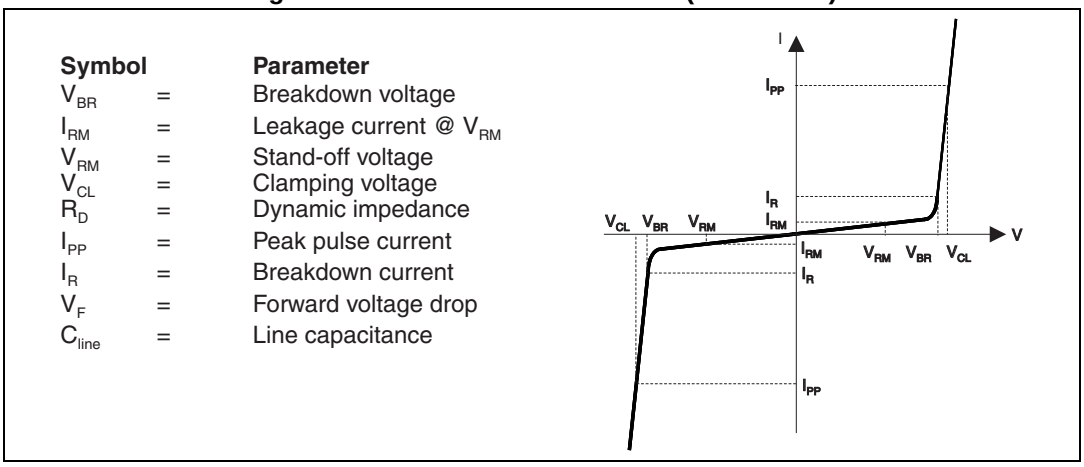


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8		V
I_{RM}	V_{RM} = 3 V per line			500	nA
$R_{I/O}$	Tolerance ± 20%		10		Ω
C_{line}	V_R = 0 V		200		pF

Figure 4. S21 (dB) attenuation measurement

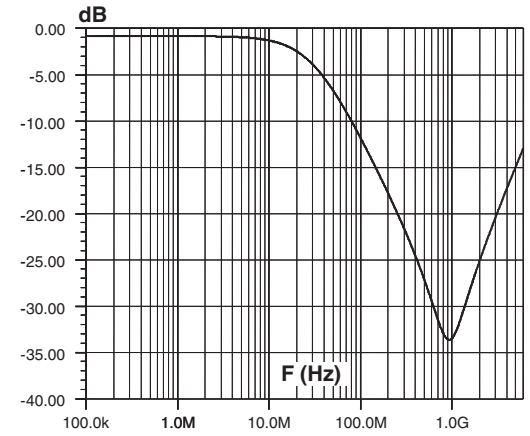


Figure 5. Analog crosstalk measurement

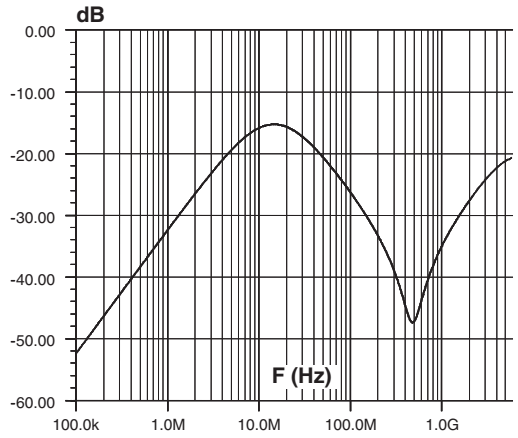


Figure 6. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input V_{in} and one output V_{out}

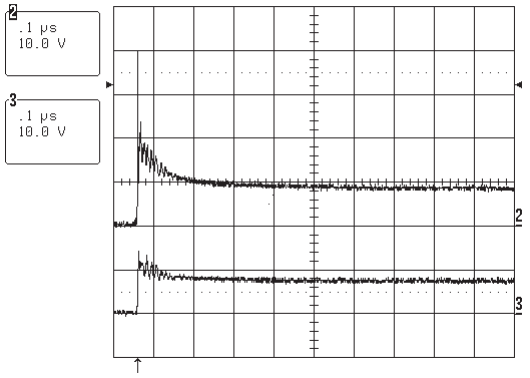


Figure 7. ESD response to IEC 61000-4-2 (- 15 kV air discharge) on one input V_{in} and one output V_{out}

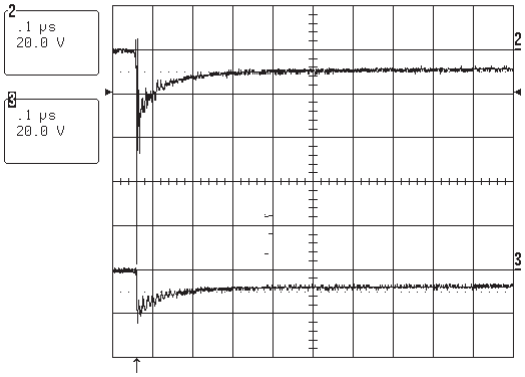


Figure 8. Line capacitance versus applied voltage

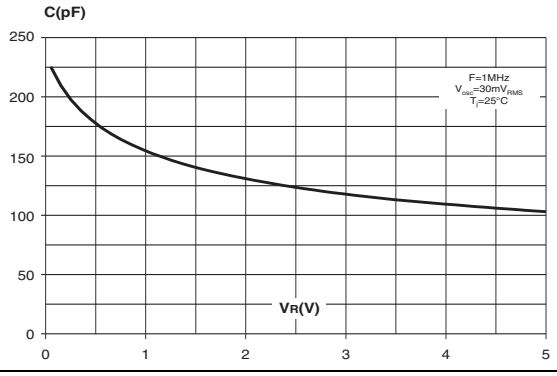


Figure 9. Aplac model

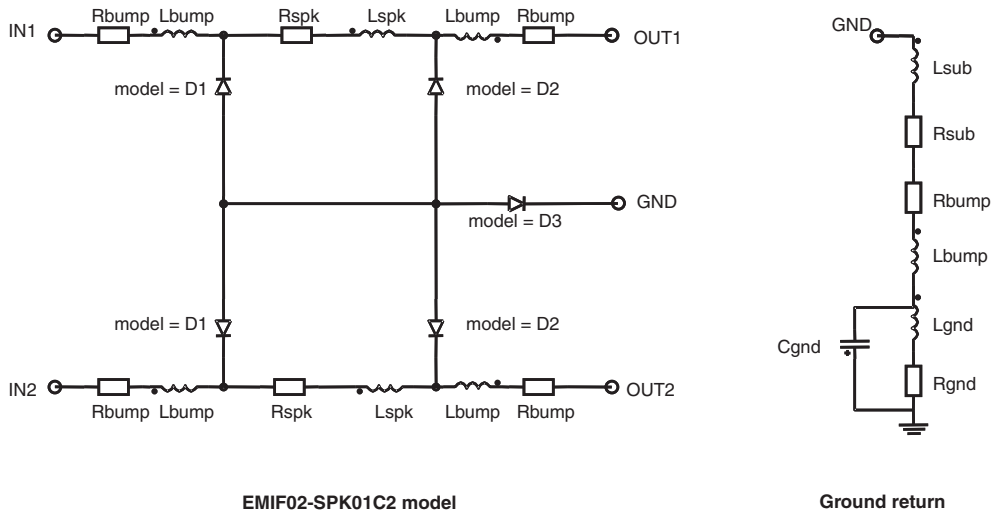


Figure 10. Aplac parameters

Model D1	Model D3	Model D2	aplacvar Ls 1nH
CJO=Cdiode1	CJO=Cdiode3	CJO=Cdiode2	aplacvar Rs 150m
BV=7	BV=7	BV=7	aplacvar Rspk 10
IBV=1u	IBV=1u	IBV=1u	aplacvar Lspk 10p
IKF=1000	IKF=1000	IKF=1000	aplacvar Cdiode1 234pF
IS=10f	IS=10f	IS=10f	aplacvar Cdiode2 3.5ppF
ISR=100p	ISR=100p	ISR=100p	aplacvar Cdiode3 1nF
N=1	N=1	N=1	aplacvar Lbump 50pH
M=0.3333	M=0.3333	M=0.3333	aplacvar Rbump 10m
RS=0.7	RS=0.12	RS=0.3	aplacvar Rsub 0.5m
VJ=0.6	VJ=0.6	VJ=0.6	aplacvar Lsub 10pH
TT=50n	TT=50n	TT=50n	aplacvar Rgnd 1m
			aplacvar Lgnd 50pH
			aplacvar Cgnd 0.15pF

2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

2.1 Flip-Chip package information

Figure 11. Flip-Chip package outline

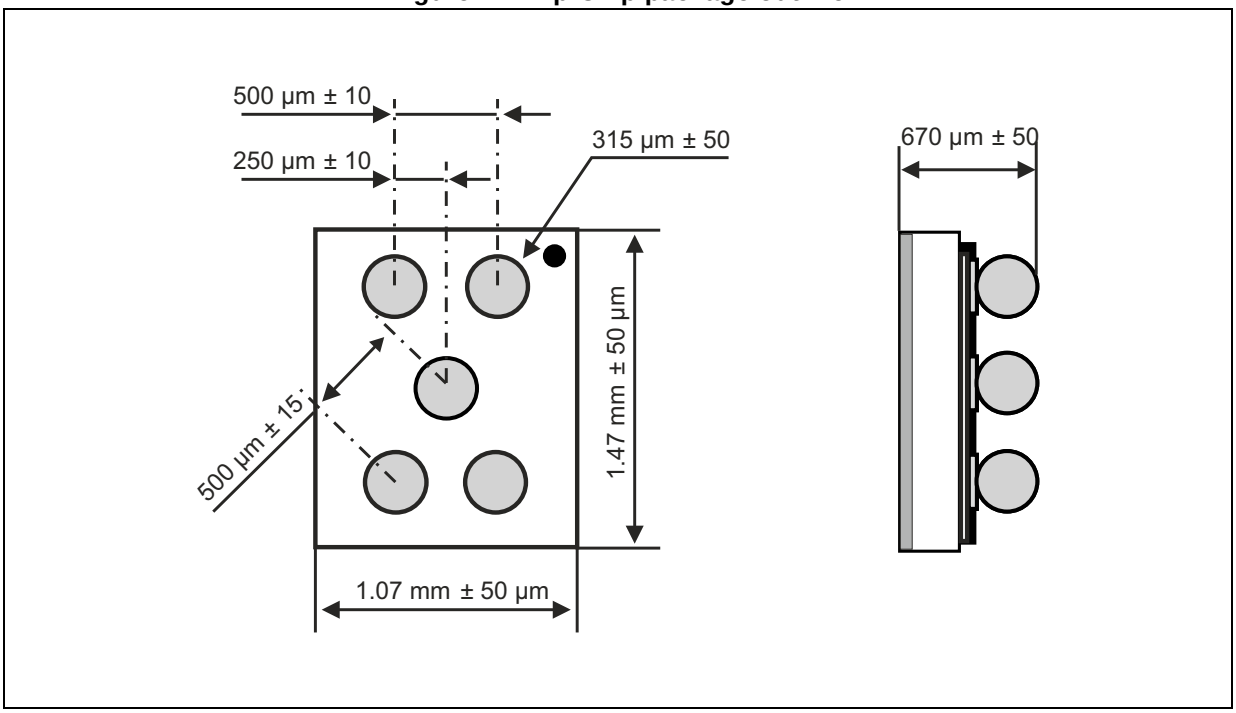


Figure 12. Marking

Dot, ST logo
xx = marking
z = manufacturing location
yww = datecode
(y = year ww = week)

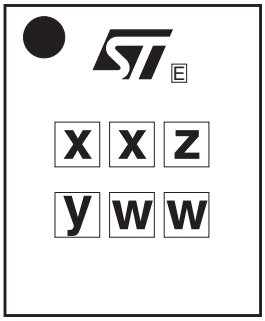
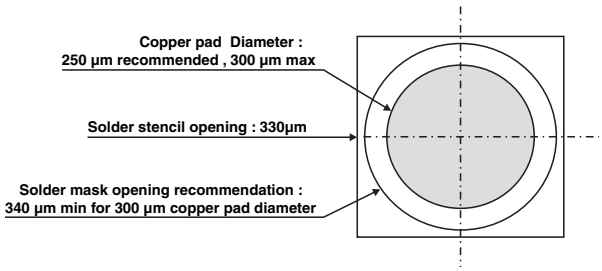
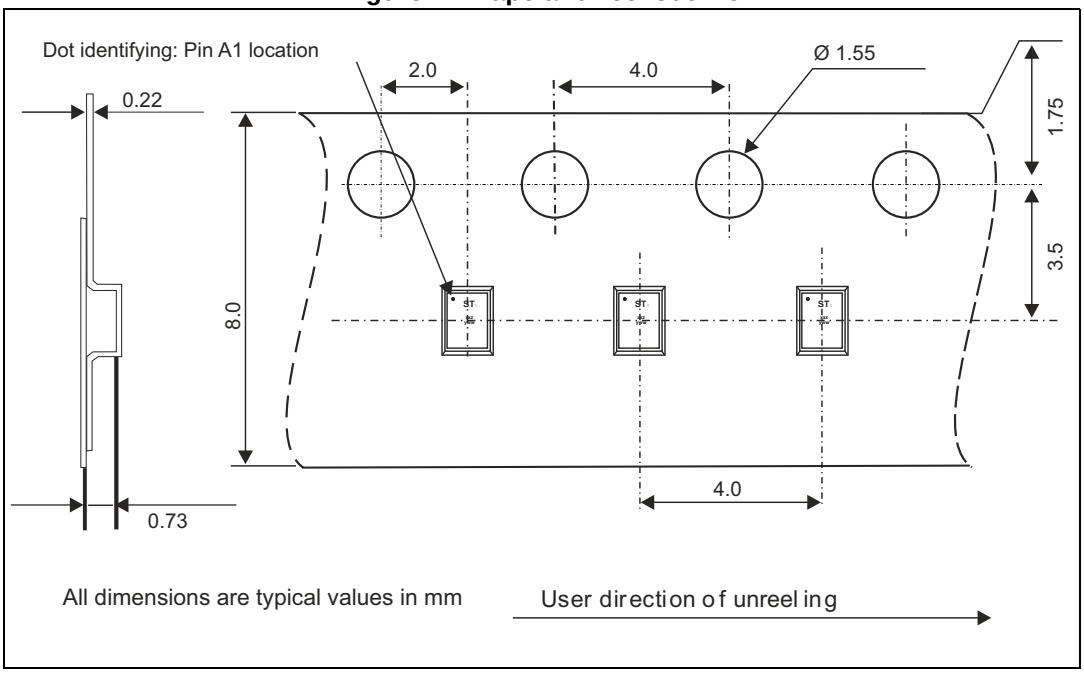


Figure 13. Footprint



2.2 Packing information

Figure 14. Tape and reel outline



3 Ordering information

Figure 15. Ordering information scheme

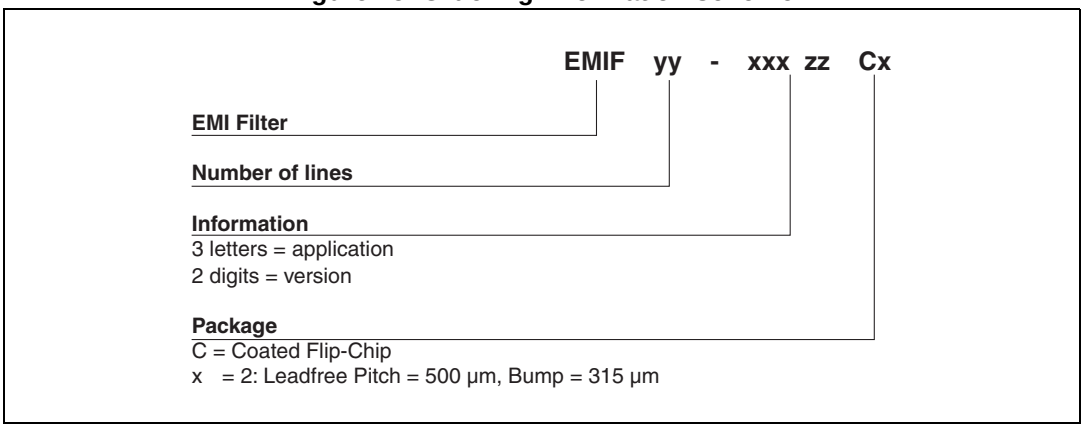


Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-SPK01C2	FX	Flip Chip	2.3 mg	5000	Tape and reel 7”

4 Revision history

Table 4. Document revision history

Date	Revision	Changes
26-Jan-2006	1	Initial release.
22-May-2013	2	Updated Figure 13.
02-Nov-2015	3	Updated *Features* and *Flip-Chip package outline*.